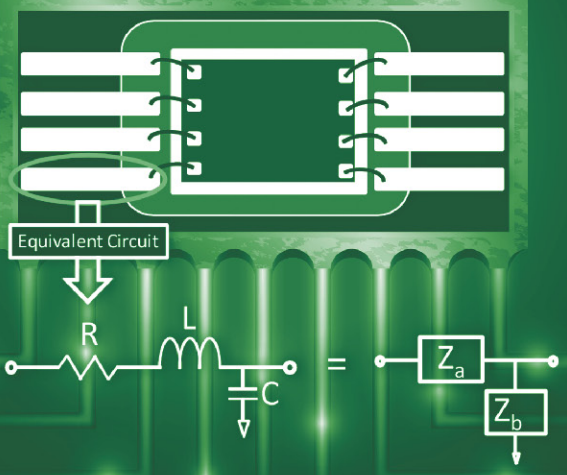
Microwave and Millimeter-Wave Electronic Packaging



Rick Sturdivant

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Microwave and Millimeter-Wave Electronic Packaging

Rick Sturdivant

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This work is dedicated to my wife, Jonie,
and my parents, Jim and Linda

Contents

	Preface	***xv***
1	**Introduction**	**1**
1.1	Distributed Effects	4
1.1.1	Distributed Effects in Lumped Elements	4
1.1.2	Undesired Resonances	6
1.1.3	Transmission Lines	10
1.1.4	Dispersion Effects	20
1.1.5	Coupling and Cross-Talk Between Signal Lines	21
1.1.6	Parasitic and Grounding Concerns	26
1.2	Thermal Effects	29
1.3	First-Level Interconnects	31
1.4	Second-Level Interconnects	33
1.5	Modules	34
1.6	Conclusions	34
	Questions	35
	References	36

2	**Materials**	**39**
2.1	Electrical Parameters and Their Measurement	41
2.1.1	Dielectric Constant	41
2.1.2	Loss Tangent	46
2.1.3	Measurement of Dielectric Constants and Loss Tangents	47
2.1.4	Metal Electrical Conductivity	56
2.2	Mechanical Parameters	58
2.2.1	Thermal Conductivity	58
2.2.2	Thermal Expansion	60
2.2.3	Stress and Strain	61
2.2.4	Young's Modulus	61
	Questions	63
	References	64
3	**Ceramic Packaging**	**67**
3.1	History of Ceramics	68
3.2	Thin-Film Ceramics	69
3.3	Advanced Thin-Film Techniques	77
3.4	Thick-Film Ceramics	78
3.4.1	Thick-Film Paste	79
3.4.2	Squeegee	80
3.4.3	Frame	80
3.4.4	Screen and Mesh	80
3.4.5	Emulsion	81
3.4.6	Desired Metal Pattern	81
3.4.7	Ceramic Substrate	81
3.4.8	Printing Machine	81
3.4.9	Etching	81
3.4.10	Postprocessing	82
3.5	Thermally Enhanced Thick-Film Processes	82
3.6	High-Temperature Cofired Ceramic (HTCC)	82
3.6.1	Slurry	83
3.6.2	Tape Casting	84
3.6.3	Punching	84

3.6.4	Via Filling and Conductor Printing	85
3.6.5	Stacking, Pressing, and Cofiring	85
3.6.6	Postprocessing	86
3.7	Low-Temperature Cofired Ceramic (LTCC)	86
	Questions	87
	References	88
4	**Laminate Packaging**	**91**
4.1	Laminate Board Fabrication	92
4.1.1	Database Review and Acceptance	92
4.1.2	Artwork Generation	93
4.1.3	Clean Layers	93
4.1.4	Pattern and Etch	93
4.1.5	Bake-Out	93
4.1.6	Oxide Treatment of Inner Layers for Adhesion	93
4.1.7	Alignment and Lamination	94
4.1.8	Drill and Deburr	94
4.1.9	Through-Hole Plating	94
4.1.10	Solder Mask	95
4.1.11	Finish Plating	95
4.1.12	Silk Screen and CNC Routing	96
4.1.13	Electrical Testing and Inspection	96
4.2	Cost of Laminates	96
4.3	Laminate Circuit Board Tolerances	98
4.4	High-Performance Laminate Materials	101
4.5	Liquid Crystal Polymer	102
4.6	Laminate Multichip Modules	103
4.7	Conclusions	104
	Questions	104
	References	105
5	**First-Level Interconnects**	**107**
5.1	Wire Bond Interconnects	107

5.1.1	Wire Bond Manufacturing	108
5.1.2	Wire Bond Reliability	110
5.1.3	Wire Bond Electrical Performance and Modeling	112
5.1.4	Straight Wire Bond Between Substrates	113
5.1.5	Wire Bond Between an MMIC and Substrate	120
5.1.6	Ground Current Parasitics in Wire Bonded Circuits	122
5.1.7	Tuning Wire Bond Interconnects	124
5.1.8	Other RF Uses for Wire Bonds	124
5.2	Ribbon Bonding	126
5.3	Flip Chip Interconnects	126
5.3.1	Types of Flip Chip Interconnects	128
5.3.2	Electrical Modeling of Flip Chip Interconnects	129
5.3.3	Parasitic Modes in Flip Chip Interconnects	135
5.3.4	Thermal Concerns for Flip Chips	139
	Questions	139
	References	140
6	**Second-Level Interconnects**	**143**
6.1	Electrical Modeling of Surface-Mount Packages	146
6.2	Inductance and Capacitance Matrix Method for Package Model Extraction	147
6.3	Coupled-π Model Method	151
6.4	Hybrid Circuit Model	157
	Questions	159
	References	159
7	**Modules and Motherboards**	**161**
7.1	Proper Transmission Line Design	162
7.1.1	Conductor-Backed Coplanar Waveguide	162
7.1.2	Striplines	168
7.1.3	Microstrip Lines	171
7.2	Vias for Isolation and Grounding	175
7.3	Cavity Resonances	176

	Questions	177
	References	178
8	**Transitions and 3D Packaging**	**181**
8.1	Transitions Between Transmission Lines	182
8.1.1	CBCPW to Microstrip Transition	183
8.1.2	Cofired Ceramic Microstrip and Stripline Transition	183
8.1.3	Laminate Board Microstrip to Stripline Transition	189
8.2	Three-Dimensional Packaging	190
8.2.1	Stacked Substrate Solderless Interconnects	190
8.2.2	Highly Integrated Modules with Vertical Transitions	195
8.2.3	Using the Package as a Circuit Element: An Integrated 60-GHz Module	196
8.2.4	Three-Dimensional Integration by Stacking ICs and Packages	196
8.3	Conclusions	197
	Questions	198
	References	198
9	**Heat Transfer**	**201**
9.1	Heat Transfer Mechanisms	201
9.2	Amplifier Efficiency and Dissipated Thermal Power	203
9.3	Reliability and Arrhenius Equation	205
9.4	Device Junction Temperature	208
9.5	Junction Temperature with Multiple Material Layers	209
9.6	Thermal Simulations Using Spice	212
9.7	Thermal Simulation Using the Finite Difference Method	213
9.8	Conclusions	216
	Questions	216
	References	217

10	**Electromagnetic Modeling**	**219**
10.1	Quasistatic Simulation of Transmission Lines	223
10.2	Method of Moments	227
10.3	Finite Element Method	228
10.4	Finite Difference Time Domain Method	228
10.5	Mode Matching Technique	229
10.6	Integrated Methods	229
10.7	Domain Decomposition Methods	230
	Questions	230
	References	231
11	**Conclusions and Future Horizons**	**233**
11.1	The 10 Keys to Successful Packaging	234
11.1.1	Careful System Architecture and Solid Specifications	234
11.1.2	Proper Material Selection	235
11.1.3	Electrical Signal Integrity	235
11.1.4	Thermal Management	236
11.1.5	Proper Electrical Modeling	236
11.1.6	Proper Mechanical Modeling	236
11.1.7	Design for Manufacturing	236
11.1.8	Design for Testability	237
11.1.9	Production Process Transition	237
11.1.10	Proper Feedback from Field Failures	237
11.2	Future for Packaging at Microwave Frequencies	237
11.3	Drive for Lower Cost Packaging at Millimeter-Wave Frequencies	238
	References	238
	Appendix A	**241**
A.1	Scattering Parameters	241
A.2	Impedance Parameters	243

Appendix B **245**

B.1 Multilayer Transmission Line Tool 245

B.2 Physical Parameters 245

B.3 Numerical Control 246

B.4 Analysis 246

Appendix C **249**

C.1 Thermal Calculator Software Tool 249

About the Author **251**

Index **253**

Preface

Packaging of electronic components at microwave and millimeter-wave frequencies requires the same level of engineering effort used for lower frequency electronics, plus a set of additional activities that are unique due to the higher frequency of operation. Without careful attention to these additional issues, it is not possible to successfully engineer electronic packaging at these frequencies. This book presents the electronic packaging issues that are unique to microwave and millimeter-wave frequencies and reviews general electronic packaging techniques for how they can be tailored to higher frequency designs.

The book chapters are organized into groups. Each chapter has a few examples, some of which are mentioned here. Two free software analysis programs are also provided and discussed in the examples. The software programs are available for downloading from www.ricksturdivant.com.

Chapter 1 begins with an introduction to the topic of packaging at microwave and millimeter-wave frequencies. Why is packaging at these frequencies so difficult? The answer to this question as well some concrete examples are given. This chapter concludes with an introduction to the concept of first-level, second-level and circuit board-level packaging.

Chapters 2, 3, and 4 address materials issues, ceramic packaging, and laminate circuit boards. These three topics are grouped together because they form the material foundation for most electronic packaging. Although the topic of materials could warrant its own volume, Chapter 2 addresses materials issues that are of particular interest for high-frequency package designs. In particular, the impacts of material choices on electrical and thermal performance are shown. Chapter 3 focuses on ceramics for packaging. It starts with a brief history of the development of ceramics and moves to thin films, thick films, and HTCC and LTCC packaging. Although ceramics are very common at these

frequencies, laminate-based packaging, which is the topic of Chapter 4, is very attractive for low-cost, high-volume products.

Chapters 5 and 6 focus on first- and second-level packaging challenges. First-level packaging includes wire bonds, ribbon bonds, and flip chips. Chapter 5 focuses on the electrical modeling of wire bonds and flip chip interconnects. Equivalent circuits are developed and modeling methods are discussed. Second-level packaging, discussed in Chapter 6, includes quad flat no-lead (QFN) packages, leadless chip carriers, and packages with leads and solder bump packages. Of particular concern is the proper modeling of package-to-motherboard transitions so several modeling methods are shown to address this.

Chapters 7 and 8 deal with modules, motherboards, transitions, and 3D packaging. Microelectronic modules and motherboards, discussed in Chapter 7, must have properly designed transmission lines to interconnect between integrated circuits, which is the main focus of the chapter. Practical design issues such as avoiding higher order modes and coupling are discussed. The chapter concludes with discussions on the use of isolation vias and avoiding cavity resonances. The focus of Chapter 8 is on transitions between signal transport structures such as transmission lines and 3D packaging interconnects. Transitions between CBCPW, microstrip, and a vertical transition between stripline and microstrip are shown. Considerable emphasis is placed on the development of a model based on closed-form equations for the microstrip-to-stripline transition. Many products are moving to 3D packaging to achieve the levels of integration required and, hence, require the use of compressible connectors for module and circuit board stacking.

Chapters 9 and 10 focus on thermal/heat transfer and electromagnetic modeling of packages. Chapter 9 starts with a review of heat transfer mechanisms, then provides details on high-power amplifier thermal modeling with the goal of maintaining device junction temperatures to ensure reliability. The chapter concludes with a discussion of thermal modeling methods and approximation techniques. Chapter 10 addresses electrical design from the perspective of using electromagnetic design tools that have been commercialized during the past 20 years. The chapter is a high-level overview of electromagnetic analysis for electronic packaging.

The book concludes with Chapter 11. The preceding chapters are tied together with a discussion of the 10 keys to successful packaging at microwave and millimeter-wave frequencies. The chapter then concludes with discussion about some of the new horizons in electronic packaging including chip scale packaging, MEMS etching techniques, and new 3D material fabrication techniques.

In the text, *radio-frequency* is abbreviated as rf and is used in the most general sense to describe electromagnetic waves up through millimeter-wave frequencies. The word *high frequency* is used in the same sense. Throughout

most of the book, dimensions are given in units of meters except in the rare case where industry standards require the use of other units.

Electromagnetic simulations were conducted using High Frequency Structure Simulator (HFSS) from ANSYS, Inc. The author would like to thank Mr. Edmond Megerdichian for developing some of the 3D images used in the figures. The author would also like to thank the various companies that graciously supplied the images and photographs that improve the practical usefulness of this work. Samantha Ronan, the developmental editor at Artech House, was very helpful, and the reviewers of the manuscript deserve special thanks for improving my initial drafts. Finally, I would like to thank all of the wonderfully talented engineers who I have had the privilege of working with and learning from throughout my career. This is especially true of the team at the Solid State Microwave Lab at Hughes Aircraft Company.

1

Introduction

Although many of the fundamental theories for radio-frequency (rf) engineering started with James Clerk Maxwell in 1873 [1], it was Guglielmo Marconi, Karl Ferdinand Braun,[1] Nikola Tesla, and Jagadis Bose who had pioneered the application of these ideas to communicating information via radio waves by the 1890s [2, 3]. Building on these accomplishments, many individuals contributed to the progress of rf technology. Then during the Second World War, the uses of rf exploded. It was applied to radar systems and proximity fuses for mortar shells.

Researchers quickly realized that the available frequency spectrum needed to be categorized and organized. Therefore, the frequency spectrum was divided into bands. Table 1.1 lists the IEEE standard band designations from 30 MHz to 110 GHz. The microwave frequency range is from 500 MHz to 20 GHz. The millimeter-wave range is from 20 to 110 GHz. Frequencies above 110 GHz are in the submillimeter-wave range.

The electronics in early rf systems used vacuum tubes and were packaged inside metal boxes with large power supply transformers, knobs, lights, and user interfaces with mechanical dials.[2] The advent of semiconductor electronics was followed by a revolution in electronic packaging. The packaging of electronics has continued to improve through new materials, processing methods, and design tools. In fact, modern electronic packaging has matured to the point that data rates that can be supported are 10^6 to 10^9 times than in the early days of vacuum tubes.

However, in these early days the title of packaging engineer and its derivatives did not exist. So, what is a packaging engineer? What is electronic

1. Marconi and Braun shared the 1909 Nobel Prize in Physics "in recognition of their contributions to the development of wireless telegraphy."
2. Vacuum tubes are still used today in traveling wave tube (TWT) amplifiers and in many high-power radio transmitters.

Table 1.1
Industry Standard Frequency Band Designations

Band Name	Frequency (GHz)
VHF	0.03–0.3
UHF	0.3–1
L-band	1–2
S-band	2–4
C-band	4–8
X-band	8–12
Ku-band	12–18
K-band	18–27
Ka-band	27–40
V-band	40–75
W-band	75–110

packaging? Electronic packaging is subset of engineering concerned with the protection, reliability, and signal integrity of electrical circuits. In most instances, electronic packaging makes the connection between integrated circuits (ICs) and the next level (such as the circuit board) that contains them. The circuit connection must be developed such that the signals from the integrated circuit are not degraded by the packaging. Also, the packaging must achieve any thermal and environmental requirements.

It turns out that most microwave and millimeter-wave engineers developing modules and circuit boards have been doing electronic packaging, but just did not know it. This is due to the fact that the design of many microwave circuits, especially modules (often called microwave integrated circuits or microwave hybrids), requires consideration of the materials being used, wire bond type and placement, IC attachment method, thermal design concerns, *and* all of the rf issues. Therefore, it was easy for many microwave designers to make the transition to "packaging engineer." About half of the packaging engineers developing microwave and millimeter-wave products have a background in mechanical engineering; the others have degrees in electrical engineering and are specialists in electromagnetics. Packaging teams are best served by having both types of engineers on board.

Modern packaging methods have been applied to lower frequency circuits such as power supplies, digital circuits, and analog circuits. However, the packaging techniques used in these lower frequencies applications cannot, in general, be applied directly to packaging at higher frequencies. This is due to factors that become important as the operating frequency increases. Even the world's most impressive millimeter-wave integrated circuit will not be usable if its packaging has not been developed to perform at those frequencies.

At lower frequencies the issues that engineers developing packaging solutions must address are fairly well understood. The concerns include:

- Materials compatibility;
- Reliability;
- Interconnects (wire bonding, soldering);
- Attachment and sealing (die attachments, encapsulation, seam sealing);
- Thermal design.

At higher frequencies a set of additional issues arises. These additional issues combine to make packaging at higher frequencies challenging. Those concerns can be summarized as:

- Distributed effects;
- Undesired resonances in packaging elements or modules;
- Circuit traces that must be treated as transmission lines;
- Dispersion effects;
- Coupling and cross-talk between circuits;
- Very high heat density in circuits, requiring exotic packaging solutions;
- Parasitic effects and proper rf grounding;
- Hermeticity or otherwise protection of the electronics.

These additional concerns are the reason why it is so difficult to package electronic components and modules at higher frequencies.

This introductory chapter focuses on some of the unique challenges that are characteristic of packaging at microwave and millimeter-wave frequencies. Also, this chapter introduces most of the concepts that will be covered in more detail in later chapters. Section 1.1 introduces the concept of distributed effects. Sections 1.1.1 to 1.1.6 provide examples and distributed effects to illustrate the important role they play in high-frequency packaging. For instance, lumped elements are discussed with a specific example of measured data for a capacitor compared to the ideal model. Next, undesired package resonances are explained and two methods are presented for calculating the lowest resonant frequency. Transmission lines are then reviewed and the insertion loss mechanisms are described. The impact of dispersion on high-speed signal lines is shown. Coupling, both desired and undesired, in transmission lines is discussed. Section 1.2 introduces some of the thermal design concerns. Finally, the chapter concludes with Sections 1.3 through 1.4 by introducing first- and second-level packaging,

modules, circuit boards, and parasitics. Finally, Section 1.6 concludes this introduction. Upon completion of this chapter, the reader should be able to skip to any chapter of interest and proceed with confidence.

1.1 Distributed Effects

In the most general sense, distributed effects are electrical performance changes that occur as the operating frequency is increased. On one hand, these distributed effects are not desired for many circuits. On the other hand, the distributed effects are very useful and allow for the creation of circuits using only patterned metal on a dielectric. Filters, for example, can be fabricated on a dielectric substrate using only a metal pattern.

Distributed effects are a result of the physical dimensions of the circuit elements being an appreciable fraction of a wavelength. Some examples of distributed effects are as follows:

- Lumped elements such as resistors, capacitors, and inductors no longer behave as lumped elements at higher frequencies without careful design.
- Metal package housings behave electrically as metal enclosed cavity resonators, causing undesired effects.
- Interconnecting signal traces no longer perform as simple wire connections, but instead must be treated as transmission lines.
- Wire bonds no longer perform as simple wire connections, but instead appear as series inductors.
- As frequencies increase, wire bonds will resonant or appear as small antennas radiating signals into the rest of the package or system.

1.1.1 Distributed Effects in Lumped Elements

To get an indication of the impact of operating at high frequencies, and the impact of distributed effects, consider one of the simplest components used in electrical circuits, the capacitor. The performance of an ideal capacitor is well known. Its reactance is

$$Z(\omega)=\frac{1}{j\omega C} \quad [\Omega] \tag{1.1}$$

where:

Z = frequency-dependent reactance of the capacitor (Ω)

$j = \sqrt{-1}$

C = capacitance of the capacitor (F)

$\omega = 2\pi f$ (rad)

f = frequency of operation (Hz).

At lower frequencies, (1.1) is completely valid and can be used with great success. However, as the operating frequency increases, the dimensions of the capacitor begin to become an appreciable portion of a wavelength, which is inversely proportional to frequency according to

$$\lambda = \frac{v}{f} \quad [\text{m}] \tag{1.2}$$

where:

λ = wavelength (m)

$v = c/\sqrt{\varepsilon_r}$ = velocity of the signal in the dielectric material (m/s)

$c = 3 \times 10^8$ m/s = speed of light in free space

ε_r = dielectric constant of the material from which the capacitor is made.

For instance, consider a standard capacitor in a 0805 package (0.08" × 0.05"= 2 mm × 1.27 mm, physical size). If the operating frequency is 10 MHz, and the capacitor is made of Al2O3 (alumina) with $\varepsilon_r = 9.8$, then the wavelength in the material is

$$\lambda(\text{at 2 MHz}) = \frac{c/\sqrt{\varepsilon_r}}{\text{f}} = \frac{3\times10^8/\sqrt{9.8}}{2\times10^6} = 47{,}915\,\text{mm}$$

$$\lambda(\text{at 2 GHz}) = \frac{v/\sqrt{\varepsilon_r}}{\text{f}} = \frac{3\times10^8/\sqrt{9.8}}{2\times10^6} = 47.92\,\text{mm}$$

At 2 MHz the capacitor is a small fraction of a wavelength (47,915 mm/2 mm = 23,957) or it is about 1/24,000th of a wavelength, which is a very small fraction of a wavelength. However, at 2 GHz, the capacitor is about 1/24th of a wavelength, which is an important fraction of a wavelength.

So what effect does this have on the performance of a capacitor as the operating frequency is increased? Figure 1.1 illustrates the effect by comparing the performance of simulated scattering parameters for a series-connected ideal

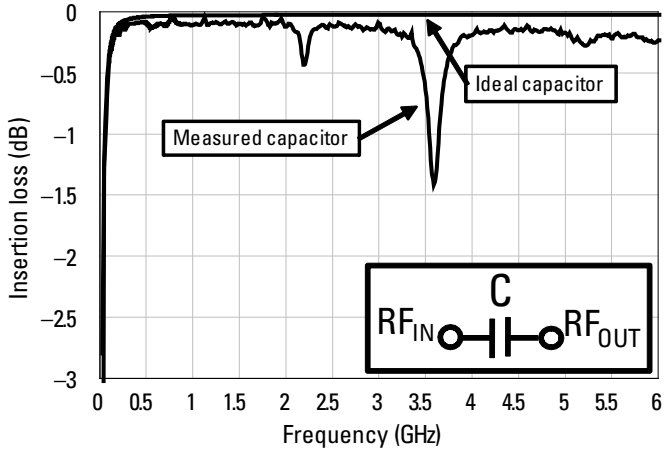


Figure 1.1 Comparison of a real and ideal capacitor showing how distributed effects begin to impact the capacitor performance above 2 GHz with C = 56 pF.

56-pF capacitor and measured data from a 56-pF, 0805 case size capacitor. Scattering parameters are described in Appendix A. It is important to note that the figure shows that both the ideal and the physical capacitor have the expected performance, which is a low-frequency open circuit, and lower insertion loss as frequency increases. However, as frequency increases, the insertion loss of the real capacitor begins to show undesired effects. In fact, at approximately 2.2 GHz, the real capacitor no longer performs as a capacitor but instead performs as a complex element with both capacitance and inductance. For most applications, this capacitor is not usable above 2 GHz since it no longer performs electrically as a capacitor.

The effect of a component's performance changing as a function of frequency (in a manner that is not linear with frequency nor consistent with low-frequency performance) is what is referred to as a distributed effect. As shown, this is due to the fact that the physical dimensions of the elements become an appreciable fraction of a wavelength.

1.1.2 Undesired Resonances

Another challenge in packaging, which is also due to distributed effects but at the package level, is undesired package resonances. The cause of these resonances is a volume that is enclosed by electric conductors to create a cavity. All metal cavities filled with a vacuum will display a resonance at a frequency given by

$$\text{Cavity resonant frequency} = f_r = \frac{c}{2a} \quad [\text{Hz}] \tag{1.3}$$

where:

c = speed of light
f_r = frequency of the resonance (Hz)
a = width of the cavity (m)

The cavity resonance predicted by (1.3) is the lowest frequency of resonance and can be a major concern for those developing microwave hybrids or microwave integrated circuits (MICs). Figure 1.2 shows a photograph of a microwave hybrid circuit. It consists of a metal housing with a ceramic substrate attached to the floor of the metal housing. The substrate can be attached with epoxy or screwed to the housing floor. The housing is made hermetic using a laser or seam sealed lid. In this case, the housing will have a resonance that, if it is in the band of operation, will significantly impact the performance of the module.

The cross section of a microwave hybrid is illustrated in Figure 1.3(a). It shows the metal box, dielectric substrate, and internal components. As can be seen in Figure 1.3(b), the electric field distribution has its peak in the middle and decays to zero and the metallic walls of the metal box. The electric field is such that it will set up a package resonance that will cause rf "suck-outs" to occur.

The lowest frequency at which the module will resonant is the most important to know and to manage. This is due to the simple fact that if the lowest resonant mode is avoided or managed properly, the other higher modes in most cases can be ignored. Thankfully, the lowest resonant mode can be calculated or

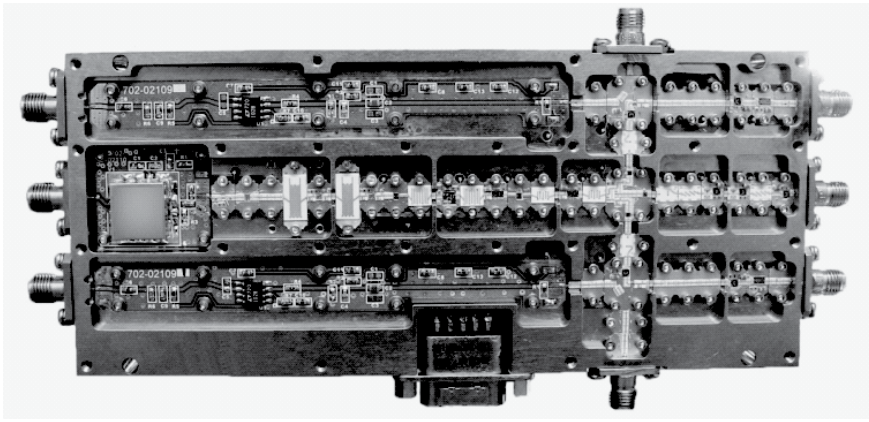


Figure 1.2 A microwave module showing components mounted to laminate substrates, ceramic substrates, and Kovar carriers inserted into metal cavities. (Photo courtesy of Norden Millimeter, Inc., Placerville, CA.)

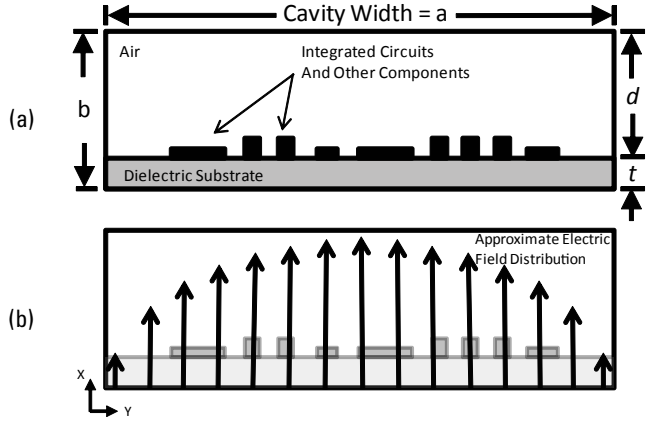


Figure 1.3 Cross section of (a) a hybrid module with a dielectric substrate and internal components and (b) the electric field distribution within the hybrid module.

approximated for most electronic models enclosed by metal walls. This can be useful to determine the proper dimensions of the housing to avoid the lowest resonance.

A first-order approximation of the resonant frequency can be achieved by ignoring the dielectric substrate and treating the cavity as a waveguide. In this case it is simple to calculate the resonant frequency using (1.3). Such an approximation will give a resonant frequency prediction that is actually higher than will be measured in the module. However, because calculation is so easily done by hand, it offers a quick assessment of resonances.

A more precise answer is usually needed that requires the dielectric substrate to be taken into account. This is achieved by recognizing that package resonance is due to the propagation of the longitudinal section magnetic (LSM) mode. In particular, it is the LSM11 mode.

A variational method can be applied to solve for the propagation constant of a dielectric filled waveguide, which will give us the desired resonant frequency of the cavity [4]. The equation for the propagation constant is

$$\gamma_{LSM11}^2 = \frac{Q}{2|P|} - \left(\frac{Q^2}{4|P|^2} - \frac{|T|}{|P|} \right)^{0.5} \tag{1.4}$$

where:

$$Q = T_{11}P_{11} + T_{00}P_{11} - 2T_{01}P_{01}$$
$$|P| = P_{11}P_{00} - P_{01}^2$$
$$|T| = T_{11}T_{00} - T_{01}^2$$

The elements of the P matrix are

$$P_{00} = 1 - \frac{\varepsilon_r - 1}{\varepsilon_r}\frac{t}{b} \tag{1.5a}$$

$$P_{01} = -\frac{\varepsilon_r - 1}{\varepsilon_r}\frac{2}{\pi}\sin\left(\frac{\eth t}{b}\right) \tag{1.5b}$$

$$P_{11} = P_{00} - \frac{\varepsilon_r - 1}{2\pi\varepsilon_r}\sin\left(\frac{2\eth t}{b}\right) \tag{1.5c}$$

The elements of the T matrix are

$$T_{00} = \left(\frac{\pi}{a}\right)^2 P_{00} - k_0^2 \tag{1.6a}$$

$$T_{01} = \left(\frac{\pi}{a}\right)^2 P_{01} \tag{1.6b}$$

$$T_{00} = \left(\frac{\pi}{a}\right)^2 P_{11} - k_0^2 + \left(\frac{\pi}{b}\right)^2 (2P_{00} - P_{11}) \tag{1.6c}$$

where:

a = cavity width (m)
b = cavity thickness (m)
t = substrate thickness (m)
d = air region thickness (m)
ε_r = dielectric constant of the substrate
$k_0 = 2\pi f/c$

f= frequency (Hz).

Setting (1.4) equal to zero and using a numerical root solving method such as the bisection technique will yield the frequency of resonance for the LSM11 mode. The independent variable in the solution algorithm is frequency, which is varied until (1.4) equals zero. This technique was implemented in a computer program and simulated for a = 12.7 mm, b = 6.35 mm, t = 0.635 mm, and a dielectric constant of 9.8. The predicted resonant frequency is 11.21 GHz.

Using the approximation from (1.3), we obtain a resonant frequency of 11.81 GHz, which is an error of about 5.3% compared to the solution from (1.4). As the substrate thickness is increased, the error from using (1.3) increases. Table 1.2 shows the effect of substrate thickness on the cavity resonance and how the error from using (1.3) increases as substrate thickness increases. In addition to the substrate thickness, as the dielectric constant of the substrate is increased, the error in using (1.3) also increases.

In practice, most modules cannot be made small enough to avoid the lowest cutoff resonance. This is especially true above 20 GHz. In these cases, a material called an *absorber* is used [5, 6]. It lowers the Q of the package resonance such that the resonance can normally be ignored. Figure 1.4(a) shows a package resonance at 7 GHz. If the module needs to perform at 7 GHz, this resonance can have a major performance impact. As can be seen, the resonance creates a "suck-out" of rf energy. Figure 1.4(b) shows the effect of adding absorber to the module. Note how the resonance is nearly eliminated by lowering its Q, where Q is the resonant frequency divided by the 3-dB bandwidth.

1.1.3 Transmission Lines

Additional distributed effects can be illustrated by considering a circuit board with signal lines. At low frequencies, the signal lines are simple wire connec-

Table 1.2
Comparison of the Dielectric Loaded Cavity Resonant Frequency Calculation Using (1.3) and (1.4) for a = 12.7mm, b = 6.35 mm, and ε_r = 9.8

Substrate Thickness, t (mm)	f_{res} (GHz) Using (1.4)	f_{res} (GHz) Using (1.3)	Error (%)
0.127	11.70	11.81	0.94
0.254	11.59	11.81	1.90
0.381	11.47	11.81	2.96
0.635	11.21	11.81	5.35
1.27	10.50	11.81	12.48
2.54	8.67	11.81	36.22

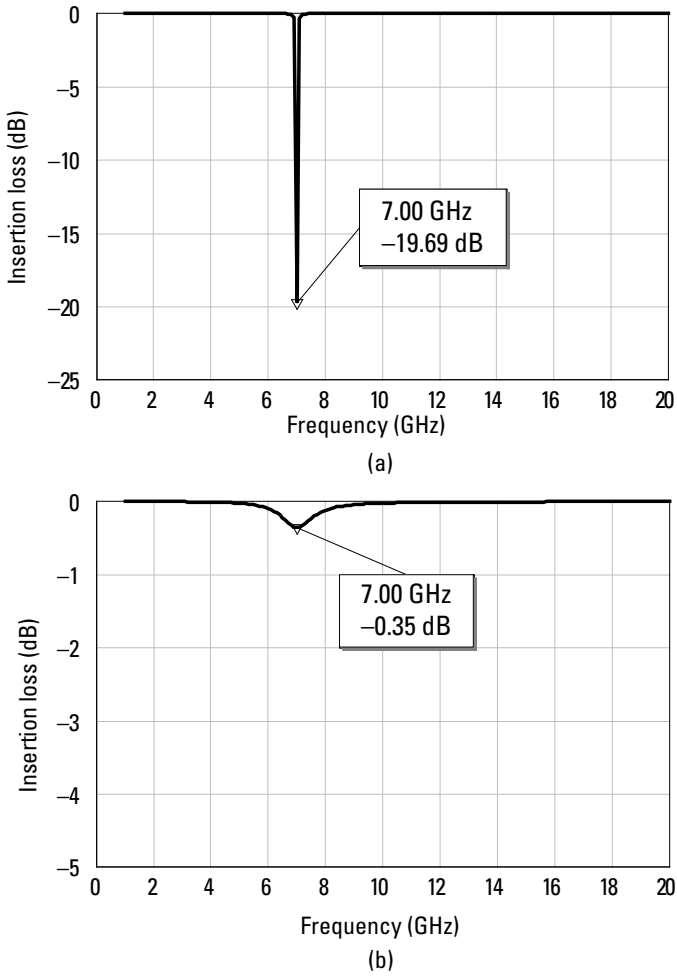


Figure 1.4 Effects of package resonance (a) without absorber and (b) with absorber.

tions between points. However, as the operating frequency increases, those signal lines behave as transmission lines. Figure 1.5 shows a representation of a transmission line. It shows a source generator V_s with a source impedance of Z_s. The load impedance is Z_L. The transmission line connects between the source circuit and the load impedance and transports the electrical signal from the source to the load. The transmission line has a characteristic impedance Z_0 and propagation constant γ that model its electrical performance.

The line impedance is a function of the dielectric material used and the feature size of the metal conductors of the transmission line. The line impedance is defined as

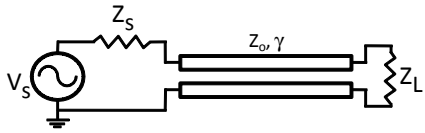


Figure 1.5 Illustration of a transmission line with line impedance Z_0 and propagation constant γ.

$$Z_0 = \sqrt{L/C} \quad [\Omega] \tag{1.7}$$

and

$$\gamma = \text{propagation constant} = \alpha + j\beta \quad [\text{rad/m}] \tag{1.8}$$

where:

L = line inductance (H/m)
C = line capacitance (F/m)
α = attenuation constant = $\alpha_c + \alpha_d$ (Np/m)
α_c = conductor loss (Np/m)
α_d = dielectric loss (Np/m)
β = phase constant (rad/m).

The attenuation constant has two components, conductive losses and dielectric losses. The conductor loss, α_c, is caused by the finite conductivity (resistance) of the metals used in the transmission line. It is important to realize that rf signals exhibit a skin effect, which causes the rf signal to only penetrate metal conductors on their surface. This effect of the signals only existing in a thin surface layer increases the insertion loss of the signal.

The skin effect can be illustrated by considering an electromagnetic plane wave incident upon a metal surface with an electric field $E_x(z)$ as shown in Figure 1.6. The plane wave induces a current J_0 on the surface of the metal. That current enters the metal and decays as illustrated in the figure due to the conductivity of the metal. The current that decays in the metal is converted into heat and is lost as conductor loss. The current, $J_x(z)$, decays exponentially as a function of the skin depth, δ. The skin depth is given by

$$\delta = \frac{1}{\sqrt{\pi \mu \sigma \text{f}}} \quad [\text{m}] \tag{1.9}$$

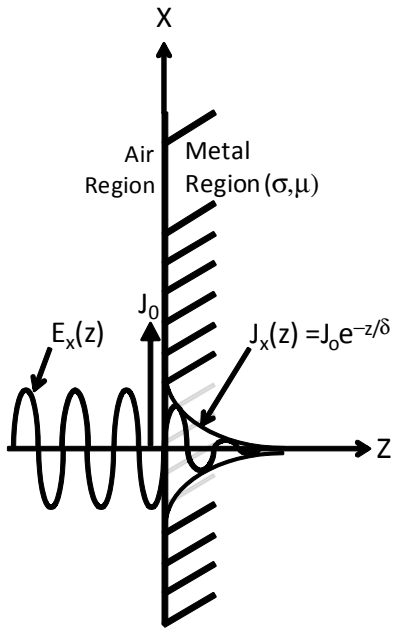


Figure 1.6 Illustration of a plane wave incident to a metal surface showing the decay of the metal into the surface of the metal.

where:

$\mu = \mu_r + \mu_0$ = permeability of the metal (H/m)
μ_r = relative permeability of the metal (H/m)
$\mu_0 = 4\pi \times 10^{-7}$ (H/m)
σ = conductivity of the metal (S/m).

The skin depths of several metals commonly used in electronic packages are shown in Table 1.3. The conductivity is given along with the skin depth in microinches and in micrometers calculated at 10 GHz. For metal plating of thin substrates, the units are often called out as microinches. It is common practice to call out a minimum metal thickness for transmission lines of 5 skin depths at the lowest expected operating frequency. At 5 skin depths, 99.3% of the current will be captured. It is important to realize that some metals, such as nickel, have a relative permeability that is greater than 1.0, which must be taken into account when calculating skin depth.

Once the skin depth is known, it is possible to determine the conductor loss since the skin depth is one of the fundamental concepts affecting conductor loss. Methods have been developed based on full-wave analysis [7], which

Table 1.3
Common Metals Used in Electronic Packaging and Their Skin Depths

Metal	Conductivity 1×10^7 (mho/m)	Skin Depth (μin.)	Skin Depth (μm)
Silver	6.30	24.96	0.634
Copper	5.80	26.02	0.661
Gold	4.10	30.95	0.786
Aluminum	3.50	33.49	0.851
Tungsten	1.79	46.83	1.190
Molybdenum	1.73	47.64	1.210
Iron	1.00	62.66	1.592
Steel	0.69	75.43	1.916

takes into account frequency-dependent effects. Full-wave methods use rigorous analyses but offer excellent agreement with measured results. Quasi-TEM methods have been developed [8] that result in closed-form equations that can be easily implemented in computer-aided design (CAD) programs. The transmission line loss analysis method that imparts a fundamental understanding is the incremental inductance rule developed by H. A. Wheeler [9–11].

The concept of incremental inductance is that the magnetic field of a transmission line penetrates into the metal, creating an internal inductance. The internal inductance, L_i, can be used to determine the loss of the transmission line. However, computation of the internal inductance can be difficult. Wheeler showed that the internal inductance can be determined from the external inductance, L_e, which is easily calculated for most transmission lines. The result is a method to determine conductor loss, α_c, based on the external transmission line inductance.

The derivation of the incremental inductance rule begins with the equation of the external inductance when the conductor is recessed by Δx. Figure 1.7 illustrates this for a coaxial transmission line. If $L_e(x)$ is the external inductance and we recess the conductor by Δx, we can write a Taylor expansion as follows:

$$L_e(x-\Delta x)=L_e(x)-\Delta x\frac{\partial L_e}{\partial x}-\Delta x\frac{\partial^2 L_e}{\partial^2 x}-\ldots \tag{1.10}$$

Now, we will assume that the recession Δx is equal to one-half of a skin depth so that

$$\Delta x=\frac{\mu}{\mu}\frac{\delta}{2} \tag{1.11}$$

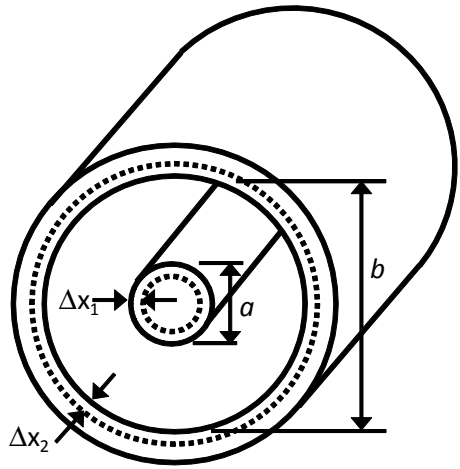


Figure 1.7 Coaxial line with the conductors recessed by $\Delta x1$ and $\Delta x2$.

If we combine (1.11) with (1.10) and we take only the first two terms of the expansion, we obtain

$$L_e\left(x-\frac{\mu}{\mu_o}\frac{\delta}{2}\right)=L_e(x)-\frac{\mu}{\mu_o}\frac{\delta}{2}\frac{\partial L_e}{\partial x} \tag{1.12}$$

The result is that we now have an equation that gives us the value of the external inductance L_e when a metal surface is reduced by a small amount (half of a skin depth). This equation can be interpreted to mean that the change in external inductance when the metal surface is recessed is equal to the external inductance before the metal surface was reduced (i.e., L_e) minus the internal inductance of the transmission line due to penetrating magnetic fields in the metal. Therefore, the internal inductance is given by the difference between the external inductance before and after the metal face is incrementally reduced, which can be written as

$$L_i=L_e(x)-L_e\left(x-\frac{\mu}{\mu_o}\frac{\delta}{2}\right)=\frac{\mu}{\mu_o}\frac{\delta}{2}\frac{\partial L_e}{\partial x} \tag{1.13}$$

which is the equation for the internal inductance. The next step is to relate (1.13) to the actual conductor loss, α_c. This is accomplished by first recognizing that the current flow in the metal generates a complex skin impedance given by

$$Z = R_{\text{skin}} + j\omega L_i \tag{1.14}$$

The complex surface impedance has equal resistive and reactive parts. Therefore, the resistive part of the surface impedance can be written as

$$R_{\text{skin}} = \omega L_i = \frac{R_s}{\mu_o}\frac{\partial L_i}{\partial x} \tag{1.15}$$

where R_s is the surface resistance $\omega\mu\delta/2$.

Finally, the actual conductor loss can be determined from the conservation of power and substation of (1.15):

$$a_c = \frac{\text{Power loss due to conductors}}{2 \text{ power transmitted}} = \frac{|I|^2 R_{\text{skin}}}{2|I|^2 Z_o} = \frac{R_s}{2\mu_o Z_o}\frac{\partial L_e}{\partial x} \quad [\text{Np/m}] \tag{1.16}$$

To determine the total insertion loss, all metal surfaces must be recessed and the contribution of each surface is summed and converting from nepers to decibels, so that

$$a_c = \frac{8.686}{2\mu_0 Z_0}\sum_{i=1}^{m} R_{si}\frac{\partial L_e}{\partial x_i} = \frac{8.686\sqrt{\varepsilon_{reff}}}{2\eta_o Z_0'}\sum_{i=1}^{m} R_{si}\frac{\partial Z_0'}{\partial x_i} \quad \left[\text{N}_\text{p}/\text{m}\right] \tag{1.17}$$

where:

x_i = the ith surface which is being recessed.
R_{si} = surface resistance of the ith metal surface
Z_0' = line impedance with the dielectric removed
η_0 = impedance of free space = 377 ohms

This method and (1.17) can be applied to the coaxial transmission line, which has a line impedance of

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}}\ln\left(\frac{b}{a}\right) \quad [\Omega] \tag{1.18}$$

In this case, the incremental inductance rule can be applied by plugging (1.18) appropriately into (1.17). The differentiation of the line impedance is with the dielectric material removed for the outer ground conductor and for the inner center conductor. Performing these steps and some results in

$$\alpha_{c,coax} = \frac{8.686\sqrt{\varepsilon_r}R_s}{2\eta_0 Z_0'}\left(\frac{\partial Z_0'}{\partial b} - \frac{\partial Z_0'}{\partial a}\right) = \frac{8.686\sqrt{\varepsilon_r}R_s}{2\eta_0 \ln(b/a)}\left(\frac{\partial Z_0'}{\partial b} - \frac{\partial Z_0'}{\partial a}\right) = \frac{13.64\sqrt{\varepsilon_r}\,\delta}{\lambda_o \ln(b/a)}\left(\frac{1}{b} + \frac{1}{a}\right) \tag{1.19}$$

which gives the conductor loss contribution to the transmission line loss. From (1.19) we can see that the insertion loss increases as the diameters of the center conductor and outer conductor are decreased. Also, the insertion loss increases as the dielectric constant of the supporting dielectric is increased and as the skin depth is increased. Keep in mind that the skin depth is inversely proportional to the square root of the metal conductivity from (1.9). Therefore, as the metal conductivity is improved, the insertion loss is also reduced.

The other contribution to transmission line loss is dielectric loss. Dielectric loss is due to dissipation of the signal in the dielectric material, which converts a portion of the rf signal into heat. For a TEM transmission line, the loss due to dielectric loss is easily calculated:

$$\alpha_d = \frac{\pi\sqrt{\varepsilon_r}}{\lambda_0}\tan\delta = \frac{\pi f\sqrt{\varepsilon_r}}{c}\tan\delta \quad \left[\mathrm{N_p/m}\right] \tag{1.20}$$

where tanδ is the dielectric loss tangent.

The dielectric loss tangent is the parameter that must be considered for each material used to support the rf signal. Many data sheets specify the loss tangent of a material or it can be measured [12–14].

Loss tangent is the tangent of the angle between the resistive component and reactive component of an electromagnetic field. If we have a time-varying electric field wave function and apply Ampere's law we obtain

$$\mathbf{E} = \mathbf{E}_0 e^{j\omega t} \tag{1.21}$$

$$\nabla \times H = \varepsilon\frac{\partial E}{\partial t} = j\omega\varepsilon' E + (\omega\varepsilon'' + \sigma)E \tag{1.22}$$

where:

$\omega = 2\pi f$(rad)

ε' = the real part of the permittivity

ε'' = the imaginary part of the permittivity due to atomic resonances.

Taking the ratio of the real part over the imaginary part of (1.22) yields the following equation for the loss tangent:

$$\tan d = \frac{\omega\varepsilon'' + \sigma}{\omega\varepsilon'} \tag{1.23}$$

Some datasheets for materials do not supply the loss tangent, but instead supply the dissipation factor. The difference between the dissipation faction and loss tangent is that the dissipation factor ignores the fact that the permittivity is complex at high frequencies due to atomic resonances within the dielectric material, $\varepsilon = \varepsilon' + j\varepsilon''$. Therefore, the dissipation factor is given as:

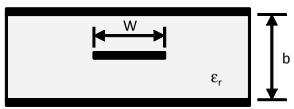
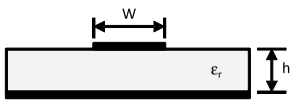
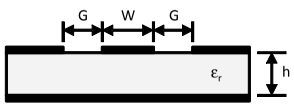
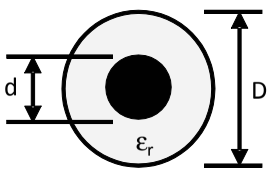
$$\text{Dissipation factor} = \text{DF} = \frac{\sigma}{\omega\varepsilon'} \tag{1.24}$$

Comparing (1.23) to (1.24) reveals that the difference is the complex portion (ε'') of the permittivity, which can be significant for some materials. However, if the loss tangent of the material is not supplied, but DF is, then it is very common to use DF directly.

Many types of transmission lines have been developed. Table 1.4 describes some of the transmission lines, their benefits, drawbacks, and typical uses. The most common transmission line may be coax. It is used to route cable television signals to homes and in high-speed networks and many other applications. Because coax has metal sleeve surrounding the dielectric, it offers excellent isolation. It also has a wide bandwidth and, ideally, zero dispersion until higher order modes begin to propagate.

The second most commonly used transmission line is probably microstrip, which is very common for circuit boards, modules, and ICs. This is mainly because of its ease of fabrication, low cost, and ease of integration with other circuits. For circuits that require buried signal lines, the choice is normally stripline. Stripline offers good isolation when properly designed with vias connecting the top and bottom grounds. Conductor-backed coplanar waveguide (CBCPW) has become a popular transmission material because it offers more isolation between adjacent circuits than does microstrip. Also, it has a lower insertion loss than microstrip.

Table 1.4
Four Common Transmission Lines Rated by Ability

Transmission Line	Isolation	Dispersion	Ease of Integration	Access to Ground	Access to Signal Line
Stripline 	High isolation especially if vias are used	Zero dispersion	Can be difficult to integrate with other components	Requires vias in the substrate to have access to ground	Poor access to signal line since it is enclosed in dielectric and outer ground
Microstrip 	Surface modes can couple to other circuits	Exhibits moderate to high dispersion depending on design	Easily integrates with other circuits	Requires vias in the substrate to have access to ground	Excellent access to signal line
Conductor-backed coplanar waveguide 	Moderate to high isolation especially if vias are used to connect top and bottom grounds	Exhibits moderate dispersion	Easily integrates with other circuits	Excellent access to ground	Excellent access to signal line
Coax 	High isolation	Zero dispersion	Easy to integrate with other coaxial components; difficult to noncoax	Excellent since ground is on the outer conductor	Poor access to signal line since it is enclosed in dielectric and outer ground

1.1.4 Dispersion Effects

Transmission lines provide an excellent method for transporting an rf signal from one location to another. Successful design of microwave and millimeter-wave packaging requires that all connecting lines and other signal conducting features be designed as transmission lines.

The frequency-dependent performance of transmission lines leads to dispersive effects. Specifically, dispersion causes the transmission line propagation constant to be nonlinear with frequency and line impedance to change as a function of frequency. In general, for narrowband systems, dispersion is not an issue. This is due to the fact that the transmission line can be designed to perform as required over the narrow band needed. However, for wideband systems, such as high-speed telecom systems, dispersion effects can significantly reduce performance.

Consider a high-speed telecom system that requires excellent eye diagram performance. Figure 1.8(a) shows a nearly ideal input eye diagram for a 40-Gbps pseudo-random binary sequency (PRBS) signal. If this signal is input into a microstrip line that is 3.81 mm (0.15 in.) long on 0.381 mm thick alumina ($\varepsilon_r = 9.8$) substrate, the output eye performance will be affected. If the input signal is sent through the microstrip line, it will become distorted as shown in Figure 1.8(b). Note the significant overshoot of the signal and the closing of the eye on the back end of the pulse. These effects are not due to impedance mismatches; they are due to the dispersion of the microstrip line.

Dispersion in a microstrip is a function of the thickness of the substrate relative to the wavelength in the substrate dielectric material. To minimize dispersion effects, the substrate thickness should be less than 5% to 10% of the wavelength in the substrate material:

$$\frac{h}{\lambda} = \frac{hf\sqrt{\varepsilon_r}}{v_o} < 0.05 \tag{1.25}$$

where h is the substrate thickness (m). Solving for substrate thickness h leads to

$$h = \frac{0.05 v_o}{f\sqrt{\varepsilon_r}} m \tag{1.26}$$

This is a convenient design guideline and it is dependent on both the substrate thickness and the dielectric constant of the substrate material. Thinner substrates and lower dielectric constant substrates result in less transmission line dispersion. The transmission line was redesigned to have a thinner substrate and lower dielectric constant. The result is shown in Figure 1.9. Note that the

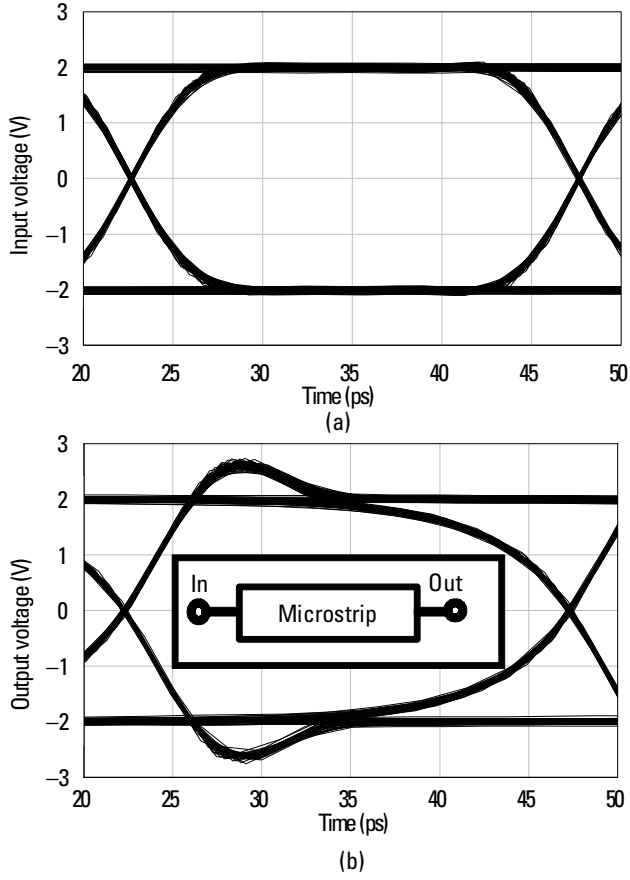


Figure 1.8 The effect of dispersion in a microstrip line can have a significant effect on high-speed communication signals: (a) Input eye diagram at 40 Gbps and (b) output eye performance after passing through a microstrip line with significant dispersion (w = 0.422 mm, L = 3.81 mm, h = 0.381 mm, and $\varepsilon_r = 9.8$).

eye diagram performance is significantly improved over that of Figure 1.8. The eye is much more open and there is very little overshoot and minimal eye closing on the back end.

1.1.5 Coupling and Cross-Talk Between Signal Lines

Coupling between circuits is a very interesting physical effect. This is partly due to the fact that it can be the source of great frustration when undesired coupling occurs in a circuit. However, it can be a very useful effect and can be used in beneficial ways for microwave and millimeter-wave circuits. An example of useful coupling is a Lange coupler [15], shown in Figure 1.10, which uses coupling between adjacent transmission lines to achieve a quadrature coupler.

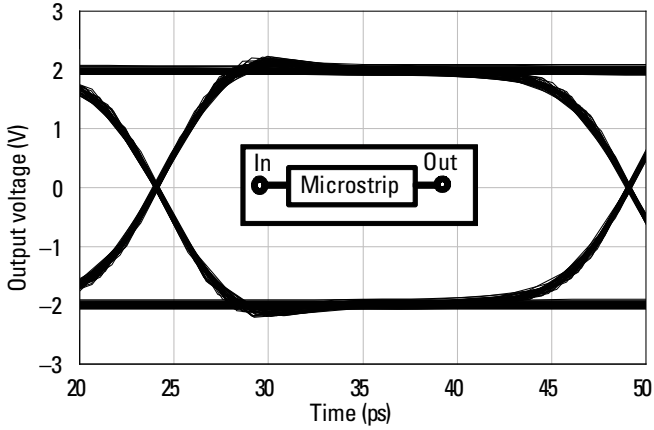


Figure 1.9 Effects of dispersion can be reduced significantly if the transmission line is properly designed as illustrated with a 40-Gbps signal that is passed through a microstrip line (w = 0.173 mm, L = 0.381 mm, h = 0.127 mm, and ε_r = 6.0).

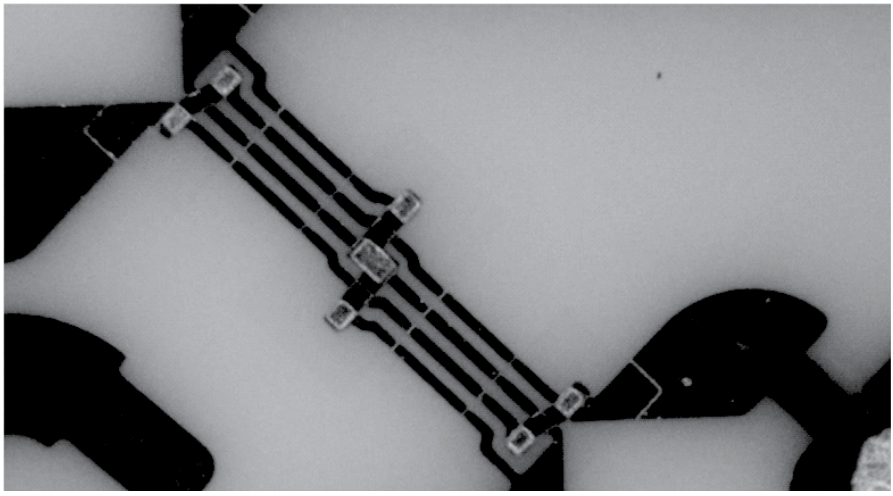


Figure 1.10 A Lange coupler fabricated in thin film with integrated signal crossover interconnects. (Photo courtesy of UltraSource, Inc., Hollis, NH.)

The coupling between the interdigitated fingers provides a 3-dB split between the outputs and the electrical length (a quarter wavelength at the operating frequency) provides the required 90-degree difference between the two output signals. Other examples of taking beneficial advantage of the coupling that occurs between transmission lines at higher frequencies include the J-coupler, interdigitated filter, and coupled line filter [16].

On the other hand, undesired coupling between transmission lines can have detrimental effects. At lower frequencies, coupling between transmission lines is treated as an effect that is linear with frequency and with the length of the line. At lower frequencies, this is a perfectly valid approach to within a few percent for many transmission lines.

A more accurate approach is to approximate the coupled lines as a capacitance that is proportional to the length of the transmission lines. Consider the plot in Figure 1.11, which shows the coupling between two parallel microstrip lines and a capacitor as a function of the length of the transmission line at 100 MHz. The length-dependent capacitor provides a highly accurate approximation to the coupling between two parallel microstrip lines.

However, as frequency increases, the coupling between transmission lines can no longer be approximated by a linear function or modeled with a simple capacitor. Consider Figure 1.12, which shows the same coupled line section as Figure 1.11, but modeled at 10 GHz instead of 100 Mhz. Note how the figure shows that the coupling is nonlinear with frequency. Therefore, the coupling must be modeled using a distributed, transmission line model.

For a coupled pair at higher frequencies, the transmission lines can be modeled by taking into account both of the zero cutoff modes, which are the even and the odd modes. Figure 1.13 shows a pair of symmetrical coupled lines.

For the odd mode, there exists a perfect electric conductor boundary condition at the line of symmetry that connects both of the capacitors $2C12$ together and to a virtual ground plane. Therefore, the distributed capacitance for the odd mode is given by

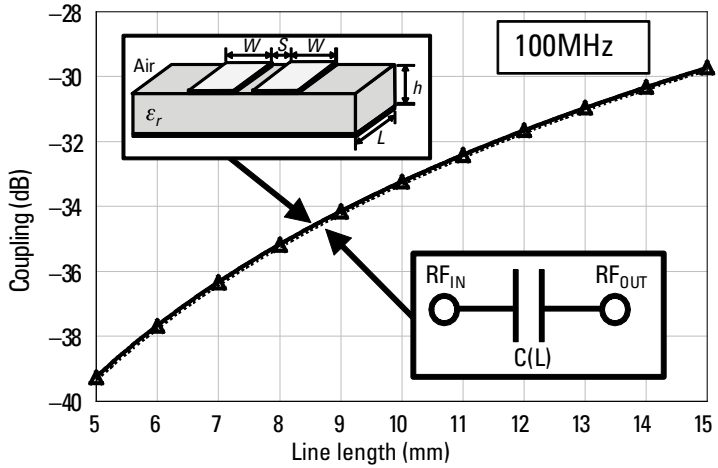


Figure 1.11 Coupling between transmission lines at 100 MHz as function of line length can be approximated by a capacitor model [$h = 0.381$ mm, $W = 0.381$ mm, $S = 0.05$ mm, $\varepsilon_r = 9.8$, and $C(L) = 0.0344 \times$ length in picofarads].

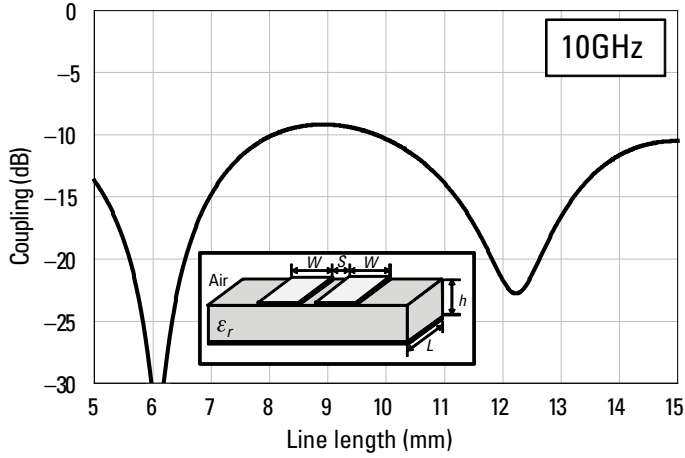


Figure 1.12 Coupling between transmission lines at 10 GHz as function of line length is more complicated and requires a more sophisticated model [$h = 0.381$ mm, $W = 0.381$ mm, $S = 0.05$ mm, $\varepsilon_r = 9.8$, and $C(L) = 0.0344 \times$ length in millimeters].

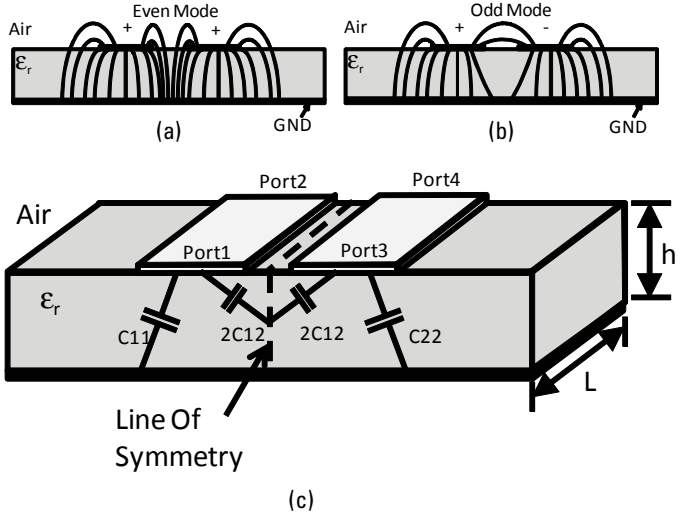


Figure 1.13 Coupled lines showing (a) the even-mode field configuration, (b) the odd-mode field configuration, and (c) the capacitance for the even and odd modes.

$$C_o = C11 + 2C12 = C22 + 2C12 \tag{1.27}$$

The odd-mode characteristic impedance is given by

$$Z_{oo} = \sqrt{\frac{L}{C_o}} \tag{1.28}$$

For the even mode, there exists a perfect magnetic boundary condition at the line of symmetry that open circuits capacitors 2C12 and removes them from the circuit. Therefore, the distributed capacitance for the even mode is given by

$$C_e = C11 = C22 \tag{1.29}$$

The even-mode characteristic impedance is given by

$$Z_{oe} = \sqrt{\frac{L}{C_e}} \text{ ohm} \tag{1.30}$$

The maximum between the transmission lines occurs when the coupled line length is a quarter wavelength (i.e., $L = \lambda/4$). If this condition is met, the coupling between the transmission lines is

$$c = \frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} \tag{1.31}$$

The coupled lines can be redrawn with the ports clearly identified as shown in Figure 1.14. Coupled lines at microwave frequencies provide maximum coupling in the reverse direction. In other words an input at Port 1 will couple to Port 3 much more strongly than to Port 4. As a result of the coupling to Port 3, insertion loss exists between Port 1 and Port 2. The insertion from Port 1 to Port 2 can also be due to many things such as losses in the transmission line due to conductor losses or dielectric losses, and there could be some radiation and there could be some loss due to reflection of energy at Port 1 due to mismatch losses. The insertion loss, due to coupling loss, is given by

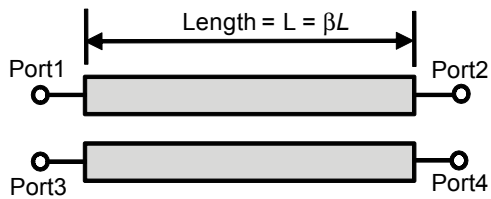


Figure 1.14 Simplified drawing of the coupled lines showing the four ports and length of the coupled lines *L*.

$$\text{Insertion loss}_{\text{Port1 to Port2}} = S21 = \sqrt{1 - c^2} \tag{1.32}$$

As an example, consider a pair of coupled lines with an even-mode impedance of Z_{oe} = 33.3 ohm, and an odd-mode impedance of Z_{oo} = 75 ohms. The maximum coupling and the maximum insertion loss due to coupling can be calculated directly using (1.21) and (1.22) as shown below. In addition, the coupled transmission lines were analyzed assuming a line length L of 10.2 mm and effective dielectric constant of 1.0 for both the even and odd modes. Figure 1.15 shows the plot of insertion loss and coupling as a function of frequency. Note the excellent agreement between the calculated and maximum coupling and maximum insertion loss:

$$\text{Coupling}_{\text{Port1 to Port3}} = S31 = c = \frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} = \frac{33.3 - 75}{33.3 + 75} = -0.384$$

$$\text{Coupling}(\text{dB}) = 20\log_{10}|c| = -8.29\,dB$$

$$\text{Insertion Loss}_{\text{Port1 to Port2}} = S21 = \sqrt{1 - c^2} = \sqrt{1 - 0.384^2} = 0.923$$

$$\text{Insertion Loss}(\text{dB}) = 20\log_{10}|0.923| = -0.695$$

1.1.6 Parasitic and Grounding Concerns

Another aspect of packaging at microwave and millimeter-wave frequencies that is unique is the concern over parasitic effects in circuits, interconnects,

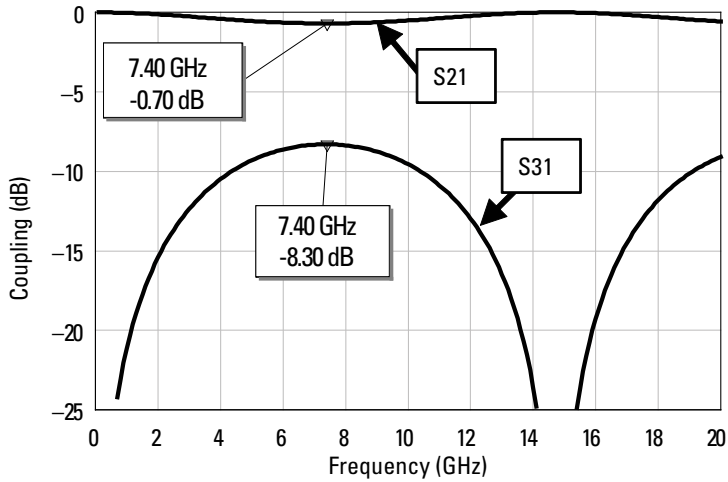


Figure 1.15 Simulated insertion loss, S21, and coupling, S31, for coupled lines that are 10.2 mm long with Z_{oo} = 75 ohms and Z_{oe} = 33.3 ohms and with effective dielectric constants equal to 1.0.

and transitions. Actually, parasitic effects in packaging can be a concern even at lower frequencies. For instance, it has been found that parasitic effects in surface-mount packages can have undesired effects at frequencies as low as a few megahertz [17]. Package parasitic resistance and inductance, resulting from the leads from the package to the motherboard, were significant enough to have an impact on electrical performance. In fact, the parasitic effects reduced the efficiency of voltage regulator modules by as much as 3.5% when the operating frequency was just 2 MHz.

However, as frequency increases, these parasitic effects become much more significant. In fact, for most microwave and millimeter-wave packages, the parasitic effects dominate the performance, such as electrical bandwidth, for electronic packaging. Consider the surface-mount package illustrated in Figure 1.16. It illustrates a very common package configuration such as an SO-8 package. In this package an integrated circuit is attached with epoxy to the paddle, and wire bonds are placed from the bonding pads on the integrated circuit to the package leads. The package is then encased in plastic using an injection process.

Figure 1.17(a) shows the top view of the SO-8-style package. Note that the illustration shows four leads as part of the package. Each of the leads from the package to the motherboard will create parasitic series inductance and resistance. Also, some shunt capacitance will exist between the leads and ground. The simplified equivalent circuit of the package parasitics is show in Figure 1.17(b).

An equation for the insertion loss of the package parasitic can be derived. The equivalent circuit can be consider the *L*-network equivalent in Figure 1.17(c) where $Z_a = R + j\omega L$ and $Z_b = 1/j\omega C$. The *Z* parameters (see Appendix A for information on *Z* and *S* parameters) can be written as

$$Z_{11} = Z_a + Z_b \tag{1.33}$$

$$Z_{22} = Z_b \tag{1.34}$$

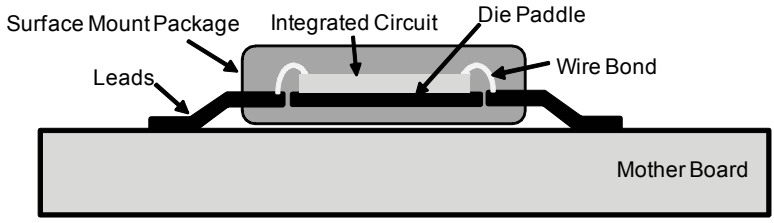


Figure 1.16 Side view of a surface-mount package. Such a package will have parasitic effects that will limit electrical performance.

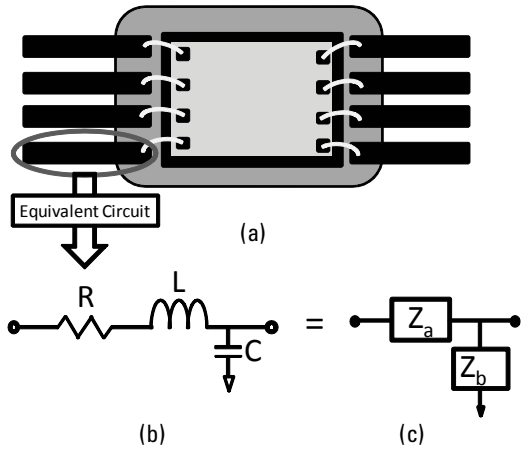


Figure 1.17 Illustration of the package showing the (a) top-down view, (b) equivalent circuit of one of the pins, and (c) the block diagram for impedance matrix analysis ($Z_a = R+j\omega L$ and $Z_b = 1/j\omega C$).

$$Z_{21} = Z_{12} = Z_b \tag{1.35}$$

Recognizing that the package will be mounted onto a substrate with transmission lines with a system impedance of Z_0, we can transform the impedance matrix into the scattering matrix for the insertion loss as follows:

$$S_{21} = \frac{2Z_0 Z_{21}}{\Delta} \tag{1.36}$$

where:

$$\Delta = \left(Z_{11} + Z_0\right)\left(Z_{22} + Z_0\right) - Z_{12}Z_{21} \tag{1.37}$$

Inserting (1.33), (1.34), and (1.35) into (1.36) and (1.37) and performing some manipulations, we can show that

$$S_{21} = \frac{2Z_0 Z_b}{\left(Z_a + Z_b + Z_0\right)\left(Z_b + z_0\right) - Z_b^2} = \frac{2}{2 + \dfrac{Z_a}{Z_0} + \dfrac{Z_a + Z_0}{Z_b}} \tag{1.38}$$

In practice, it is rare to use (1.38) in the analysis of the package. However, it is very useful to examine it to determine the effects of the parasitics on the performance of the package. Clearly, since $Z_a = R+j\omega L$, as R, L, or frequency increases, the insertion loss degrades (becomes less than 1). In addition, since $Z_b = 1/j\omega C$, as the capacitance or frequency is increased, the third term in the

denominator increases, which further degrades the insertion loss. From this it is easy to conclude that the parasitic effects degrade the high-frequency performance of the package, which is normally the situation.

Furthermore, the equivalent circuit is a simplification to make the analysis more manageable. A more realistic equivalent circuit will include effects from coupling between the pins, which can be represented as a capacitance between the pins. Also, the effect of the wire bond should be included in the model of the package. Depending on the fidelity required in the model, other elements will also need to be included.

In practice, the impact of the package parasitics leads and motherboard are measured or modeled using a 3D electromagnetic simulator and then the parasitic elements are de-imbedded. The resulting electrical model can then be used in circuit simulation.

For the package and equivalent circuit in Figure 1.17, it was found that the inductance $L = 1.4$ nH, the series resistance $R = 0.5$ ohm, and the shunt capacitance was $C = 0.6$ pF. We want to determine insertion loss as a function of frequency and the 3-dB bandwidth.

The equivalent circuit was input in a circuit simulator and the results are shown in Figure 1.18. The 3-dB bandwidth is approximately 7.7 GHz.

1.2 Thermal Effects

Heat dissipation is a concern for packaging of many electronic components. However, the thermal challenges with packaging microwave and millimeter-wave electronics are significant. This is due to the heat dissipation and power

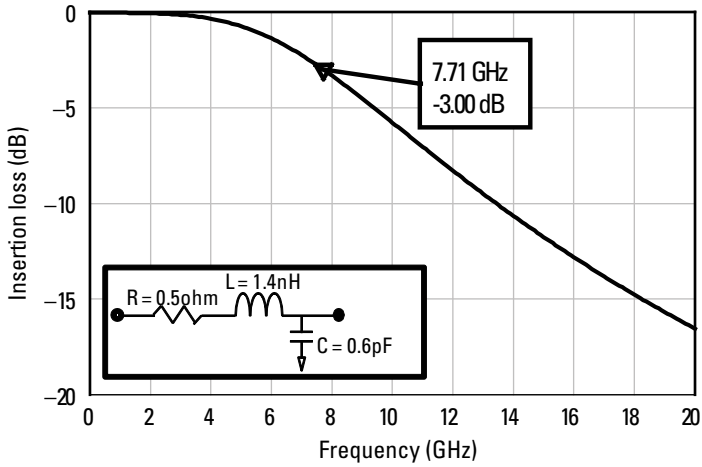


Figure 1.18 Insertion loss of the package equivalent circuit.

density of most rf high-power amplifiers. Lower frequency electronics have power densities that are typically 1 to 30 W/cm2 [18]. However, rf amplifiers can have power densities that are 200 to 2,500 W/cm2. In addition, for most lower frequency parts fabricated in complementary metal-oxide semiconductor (CMOS), the heat-generating parts are evenly distributed over the face of the integrated circuit. This is not the case for most high heat-dissipating microwave integrated circuits. Instead, the heat-generating components are normally clustered together for electrical performance reasons such as to achieve the highest output power. To illustrate this point, consider the energy density more commonly known as heat flux:

$$\text{Heat flux} = q'' = \frac{Q}{A} \quad \text{W/m}^2 \tag{1.39}$$

where:

q'' = heat flux (W/m^2)
Q = Power or the heat energy generated (W)
A = area over which the heat energy is leaving the heat source (m^2).

Now, consider the GaN high-power amplifier shown in Figure 1.19. It has a die size that is 4.57 mm × 3.6 mm with components distributed over the face of the die. Note from the figure how most of the heat-dissipating components are concentrated in one area. In this case, the field effect transistors (FETs) are connected tightly together to achieve the highest output power possible. The high-power output stage transistors cover an area that is approximately 0.45 mm × 3.6 mm. The power dissipated by the transistor is 38W. Therefore, the energy density at the bottom of the integrated circuit just under the FET devices can be calculated using (1.39) as follows:

$$q'' = \frac{38W}{0.36cm \times 0.045cm} = 2345 \quad \text{W/cm}^2$$

Therefore, careful attention must be paid to the proper selection of materials and manufacturing processes to maintain a junction temperature that is within the limits of the manufacturer.

To obtain a very practical understanding of what this level of power dissipation means, consider a common household clothes iron. Most clothes irons dissipate about 1,500W of energy when turned to their highest setting over an area that is about 25 cm × 12 cm. This results in a power density that is about 5 W/cm^2. Therefore, the power density of the high-power amplifier output

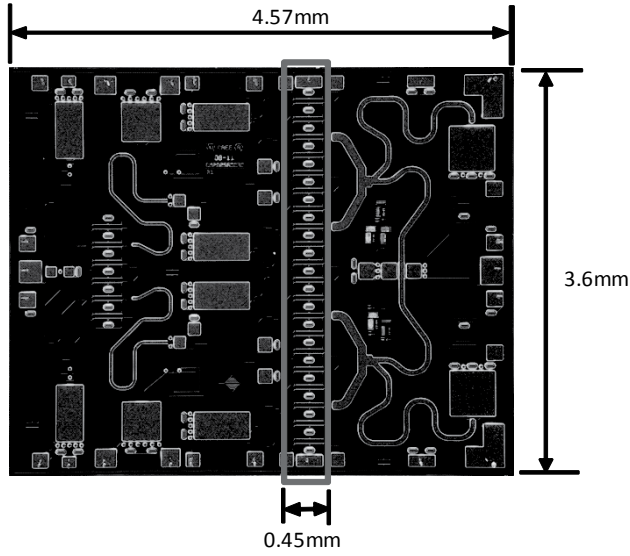


Figure 1.19 GaN high-power amplifier (HPA) with 25W of output power in the 2.5- to 6-GHz frequency range. (Photo courtesy of Cree, Inc., Durham, NC.)

FETs is about 600 times higher than that of a clothes iron turned to its highest power setting!

The manufacturer's data sheet for this GaN amplifier suggests that it be attached using AuSn (80/20) to a copper tungsten (CuW) carrier. This arrangement is sketched in Figure 1.20. It is important for the AuSn eutectic attachment to be void free so that the maximum thermal path exists between the GaN die and the CuW heat spreader. Note that any voids present in the AuSn attachment can result in a large temperature rise due to the magnitude of the previously mentioned heat flux. Normally, the attachment is done in a vacuum and with AuSn performs that are fabricated specifically to match the dimensions of the die. In addition, a fixture is normally required to achieve reliable void-free attachment. The fixture, often machined from graphite, aligns the die with the heat sink. In addition, the fixture maintains pressure on the die to realize the required AuSn squeeze-out and eliminate voids. The resulting die-to-heat sink subassembly is then integrated into a module package.

1.3 First-Level Interconnects

First-level interconnects (FLIs) are the electrical connections between semiconductor devices such as integrated circuits or transistors and the first level of packaging. The most familiar and widely used FLI is the wire bond. Wire

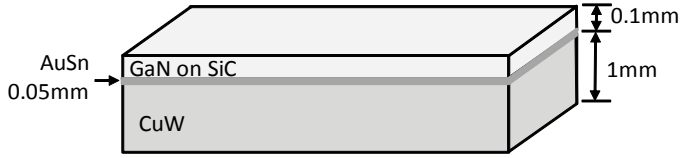
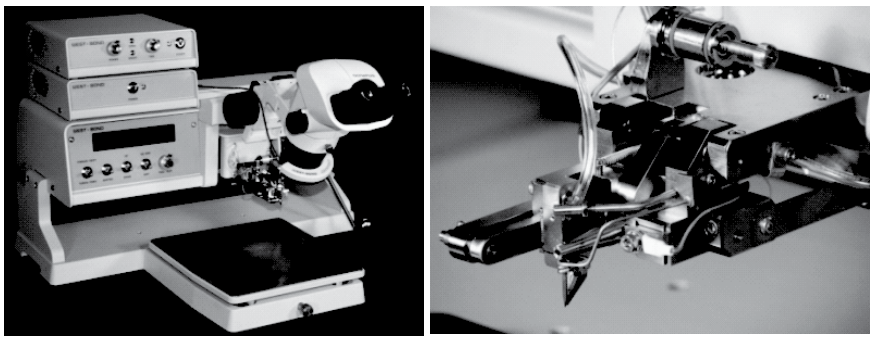


Figure 1.20 GaN monolithic microwave integrated circuit (MMIC) is attached to a CuW heat spreader using AuSn solder.

bonds are available in several types, such as ball bonds, wedge bonds, and ribbon bonds, each with unique variations. Some examples of FLIs are:

- Wire bonds;
- Ribbon bonds;
- Flip chips using hard bumps;
- Reflow solder ball connections;
- Z-axis films;
- Epoxies.

An example of a wire bond is shown in Figure 1.21(a). The wire bond is formed using a gold wire that is typically 0.025 mm in diameter, though high-volume commercial systems at lower frequencies use aluminum wire bonds with diameters as large as 0.254 mm. Figure 1.21(b) shows a machine for manufacturing wire bonds. It is a manual wire bonder, and a properly trained operator can use it to place highly reliable wire bonds.



(a) (b)

Figure 1.21 The most common interconnect is the (a) wire bond and it is placed using (b) wire bonding machines that are able to place wire bonds with precision down to a few micrometers. (Photos courtesy of WestBond, Inc., Anaheim, CA.)

Wire bonds can be connected using ultrasonic bonding, thermocompression bonding, and thermosonic bonding. Ultrasonic bonding uses pressure and ultrasonic vibrations from a bonding tool to create the bond between the wire and the metal surface. Thermocompression uses pressure from the bonding tool and high temperature to create the bond. Thermosonic bonding combines ultrasonic and thermocompression methods to create the bonds.

The purpose of the wire bond is to create an electrical connection between an integrated circuit and some type of conductor, typically a metal trace. At lower frequencies the wire bond performs as a simple electrical contact between points and is specified at a maximum current handling. However, as frequency increases, wire bonds begin to perform as inductors. Above some frequency, the wire bonds can perform as a resonator or an antenna. The requirements on the wire bond increase as frequency is increased. Typically, the length of the wire is limited to reduce inductance. Also, the shape of the wire bond is specified.

1.4 Second-Level Interconnects

Second-level interconnects (SLIs) exist between a chip package and a motherboard. For instance, consider a quad flat no-lead (QFN)-style package mounted onto a motherboard. Figure 1.22 shows a package mounted onto a printed circuit board (PCB). Normally, the interconnection is achieved using solder paste, which is screen printed onto the motherboard using a stencil. The package is then placed onto the motherboard over the screen-printed solder paste. The assembly is then sent through a solder reflow process, which is most often a multizone oven.

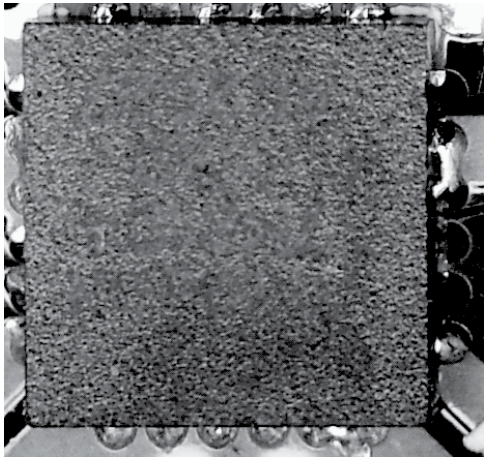


Figure 1.22 A QFN is solder attached to a motherboard.

The packaging of SLIs involves several very stable and well-understood processes. Those processes apply to both lower frequency and higher frequency packaging. A few concerns, however, are unique to microwave and millimeter-wave packaging. For instance, the motherboard metal traces connecting to the package rf pins must be designed as transmission lines with controlled impedances. The package connecting pads must be designed with the motherboard in mind to maintain an impedance match in the frequency range required. Another concern is that the grounding pedestal, which is normally at the bottom of the package, must be grounded on the motherboard with enough vias to avoid resonances.

1.5 Modules

Modules normally contain rf, control, and bias integrated circuits and passive circuits. Figure 1.23 is an image of a transmit/receive module that uses GaN high-power amplifier MMICs, a GaAs low-noise amplifier, a switch, a limiter, and bias circuitry. The substrate is fabricated from low-temperature cofired ceramic (LTCC). The high-power amplifier uses CuMo heat spreaders to improve the heat transfer from the HPA MMICs. The module output power was measured as 32W at 11 GHz and the module efficiency was 24%. The output power was more than 20W over a 1.6-GHz bandwidth. The receiving gain was measured to be 13 dB with a noise figure of 2.2 dB.

1.6 Conclusions

Clearly, many effects are critical when creating effective electronic packaging at microwave and millimeter-wave frequencies. These challenges are, for the most

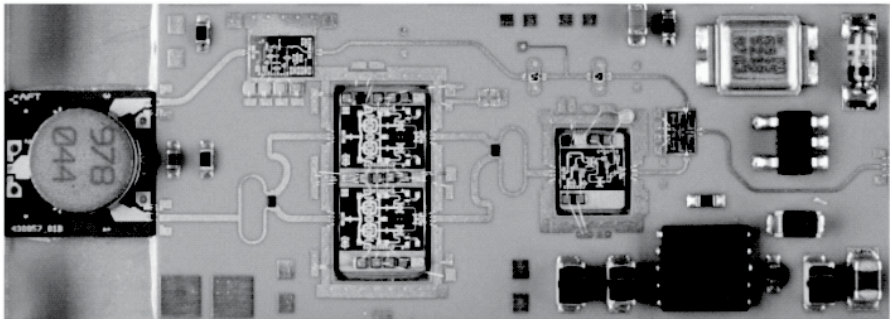


Figure 1.23 GaN transmit/receive module containing rf integrated circuits, bypass capacitors, and a ceramic substrate. (Photo courtesy of CASSIDIAN, Ulm, German. See [19].)

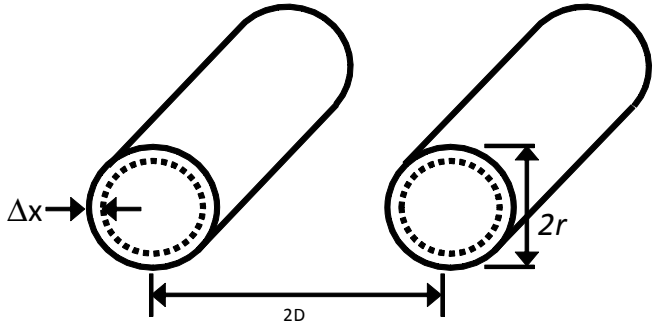
part, less important or less significant at lower frequencies. The most important concerns result from distributed effects and high thermal heat density. The difficulties that arise from distributed effects can manifest in several different ways, as introduced in this chapter. The high dissipated heat density very often determines the materials and cooling approach. Most of the topics introduced in this chapter will be discussed in much more detail in the following chapters.

Questions

1. Measured data for a lumped-element capacitor is shown as Figure 1.1. In it, resonances are apparent at 2.2 and 3.6 GHz. Develop a circuit that modifies the simple lumped-element capacitor model and correctly accounts for these resonances.
2. Measured data for a lumped-element capacitor are shown in Figure 1.1. In it, the insertion loss of the capacitor increases as frequency increases. Develop a circuit that modifies the simple capacitor model to predict the insertion loss shown.
3. What is the wavelength at 20 GHz in a dielectric with $\varepsilon_r = 9.8$? What fraction of a wavelength is a 0805 capacitor in this material at 20 GHz?
4. Using either a computer programming language or mathematical analysis software, predict the resonance of a microwave module that generates the LSM11 mode assuming a cavity width of 10 mm, cavity thickness of 6.35 mm, substrate thickness of 0.5 mm, and a dielectric constant for the substrate of 9.8. Compare this calculation to that obtained using the simple approximation in (1.3) and calculate the error.
5. Generate a curve of the current density and percentage of current density reduction as a function of the number of skin depths for copper, gold, and aluminum metal.
6. The figure below shows a two-wire transmission line. Using the incremental inductance rule, derive the equation for the conductor loss, a_c. Assume the line inductance = $L = \frac{\mu_o}{\pi} \cosh^{-1}\left(\frac{D}{r}\right)$

7. Plot the conductor loss and dielectric loss of a coaxial transmission line that is 3m long as a function of frequency from 0.5 to 100 GHz. Does the dielectric loss become more significant than the conductor loss? If so, at what frequency?

8. Generate a plot of the recommended substrate thickness to avoid dispersion problems for a 40-GHz signal as a function of substrate dielectric constant.
9. A package contains 0.0254-mm gold wire bonds with 25-GHz signals.



The wire bonds are 1 mm long. Calculate the amount of capacitance required to achieve a return loss of 20 dB at the operating frequency. Assume that the capacitance forms a lowpass-type of matching structure.

10. What is the heat flux at the bottom of an MMIC chip that is 2 mm × 2.5 mm and dissipates 4W of heat?
11. What are the differences between ultrasonic bonding, thermocompression bonding, and thermosonic bonding?
12. What is the difference between first-level and second-level interconnects?

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2

Materials

Materials used in electronic packages must be chosen carefully and the material parameters that impact performance must be understood. The decision on which materials to use occurs early in the development of a new product. Figure 2.1 illustrates a simplified material selection process that is a subset of the overall product development process. Choosing the right material starts with an understanding of the requirements of the packaging. The product requirements document must state the parameters that are affected by the choice of materials such as maximum junction temperature, hermeticity, maximum operating frequency or maximum data rate, package size, package weight, first- and second-level interconnects, and insertion loss of interconnects. Once these requirements are known, a product concept can be developed. Usually, the product concept is based on the experience of the engineer, who must balance many different variables and choose an optimum solution.

After the product concept is complete, a list of materials used in the product can be developed. The list of materials is often called the material set. For each material set, accurate material parameters must be determined. Electrical and mechanical parameters are often specified in supplier data sheets. However, this information may not exist or may be measured under conditions that are not consistent with the operating range of the product. For instance, the dielectric constant of a material may be specified at a very low frequency such as 1 MHz, but the product may need to function from 22 to 28 GHz. For microwave and millimeter-wave packaging, more often than not, materials data is not readily available at the frequencies of interest for most materials. This is

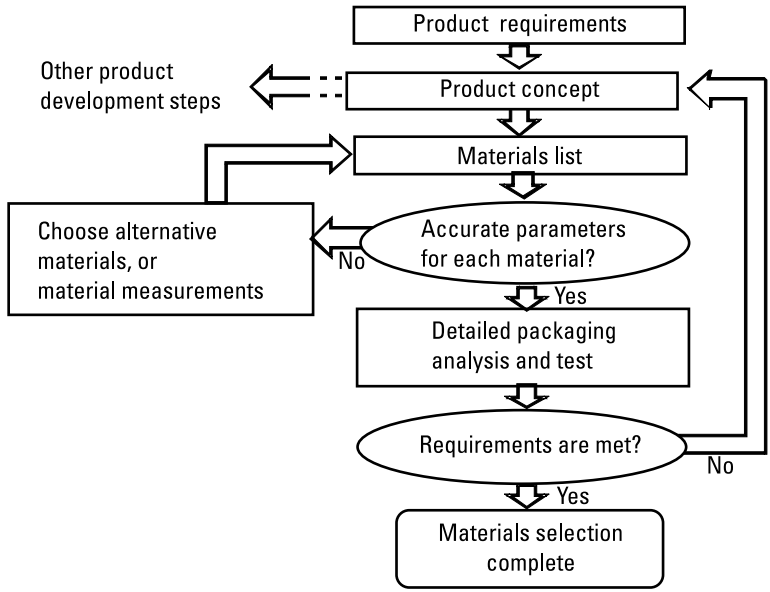


Figure 2.1 Top-level view of the material selection process for RF electronic packaging.

an example of an added level of complexity for packaging at microwave and millimeter-wave frequencies.

It is not advisable to use a material for which the relevant material parameters are unknown. Therefore, a choice must be made between either selecting an alternative material or performing materials measurements. Because of the frequent lack of dielectric constant and loss tangent data at RF frequencies, several methods have been developed to measure them. Those methods are discussed in this chapter.

Detailed analysis and testing of the product will determine whether the material set meets the requirements. The analysis usually includes circuit simulations, electromagnetic simulations, thermal analysis, and mechanical simulations. It is common for high-frequency products to have a portion or portions of the product fabricated and tested against relevant requirements to determine compliance. Ultimately, the final product is subjected to detailed design verification and reliability testing. The test results will show that the product is or is not compliant. Until the product meets requirements, the material selection process is not complete, and if compliance is not achieved the product development process may need to be restarted.

The material topics discussed in this chapter are organized into the electrical and mechanical parameters that must be considered when developing electronic packaging for a product.

2.1 Electrical Parameters and Their Measurement

As mentioned earlier, the process of choosing materials starts early in the packaging effort and includes selection based on electrical criteria. A few of the electrical material parameters are as follows:

- Dielectric constant for substrates and insulators;
- Loss tangent for substrates and insulators;
- Semiconductor conductivity and dielectric properties;
- Electrical conductivity for circuit traces and metallic features.

The electrical (and some mechanical) differences between insulators, semiconductors, and metals result from the electron energy bandgap between the valence and conduction bands [1] as shown in Figure 2.2. For dielectric materials, the energy gap between the valence and conduction bands is usually larger than 5 eV. For semiconductors, the electron gap is about 1 eV. For conductors, there is no energy gap between the valence and conduction bands and it contains free electrons.

2.1.1 Dielectric Constant

The majority of dielectric materials are characterized as being poor conductors of electric current and, equivalently, good electrical insulators. To properly understand the electric properties of dielectric materials, consider a dielectric that is placed in an electric field. Polarization occurs within the material at the microscopic level. The average equilibrium positions of bound positive and negative charges experience a displacement due to the electric field. This causes an electric dipole moment to exist in the material that affects the electric field. This effect is illustrated in Figure 2.3.

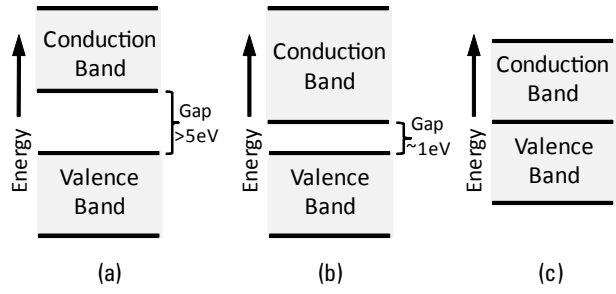


Figure 2.2 Energy bands for different types of materials: (a) insulator, (b) semiconductor, and (c) conductor. (*After:* [1].)

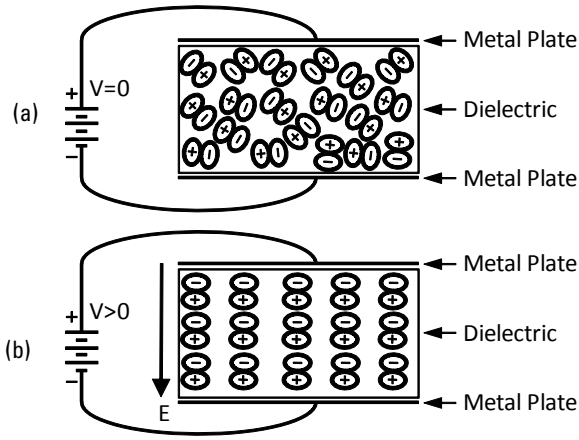


Figure 2.3 A dielectric material (a) with zero voltage on the plates will not generate an electric field in the material, but (b) when an electric field is generated the dielectric will exhibit dielectric dipoles. A dipole is a pair of charges of equal and opposite charge that are separated by a very small distance. If the electric field is removed, the dipole moments relax to the prior, random orientation.

There are three possible physical mechanisms that will generate a polarization in a dielectric material and in an electric dipole moment:

1. *Atomic polarization* occurs when the center of the electron cloud of an atom is displaced relative to the center of the nucleus in the presence of an electric field. This is the mechanism for most dielectrics used in microwave and millimeter-wave packaging.
2. *Ionic polarization* occurs when molecules with ionic bonds have a displacement of the positive ions relative to negative ions in the presence of an electric field. Common table salt, NaCl, molecules are an example.
3. *Orientation polarization* occurs when molecules that have a permanent dipole moment, but are naturally randomly oriented, orient themselves in the presence of an electric field. An example of this is water molecules, which have approximately a 104-degree angle between the two positively charged hydrogen atoms relative to the negatively charged oxygen atom.

Figure 2.4(a) shows a dielectric material in the presence of an electric field. The reaction of the dielectric to the electric field is that dipole moments are generated. For the case of atomic polarization, the electron cloud displacement creates the dipole. If a material easily aligns itself and creates a relatively large density of dielectric dipole moments, then the electric susceptibility, χ_e,

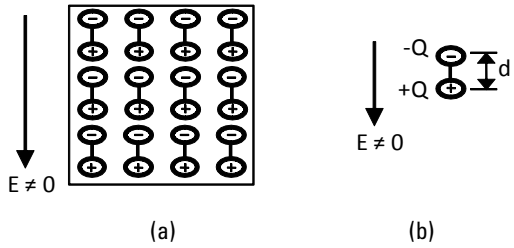


Figure 2.4 In the presence of an electric field that is not zero, (a) the dipoles line up, and (b) a displacement vector, *d*, exists between the +Q and –Q charges.

will be large. Susceptibility is the measure of a material's ability to react to the electric field by creating dipole moments. It is helpful to define the dipole moment density. The dipole density vector (pointing from negative to positive charge) can be thought of as the net dipole moment density within some volume and is given by

$$\mathbf{P} = NQ\mathbf{d} = \chi_e \varepsilon_0 \mathbf{E} \tag{2.1}$$

where:

$\mathbf{P}$ = dipole moment density

Q = charge

$\mathbf{d}$ = displacement vector between the positive and negative charges in the dipole moment

N = number of dipole moments per unit volume

χ_e = electric susceptibility of the dielectric material (how easily dipole moments are generated)

ε = permittivity

$\mathbf{E}$ = electric field.

Equation (2.1) tells us that net dipole moment density is simply the number of dipoles generated multiplied by the dipole charge multiplied by the distance between the charges. Therefore, the dipole moment density can be increased by either increasing the number of dipole moments or the distance between the charges. To determine the dielectric constant, consider the electric field displacement from Maxwell's equations; we know that

$$\mathbf{D} = \varepsilon_o \mathbf{E} + \mathbf{P} = \varepsilon_o \mathbf{E} + \varepsilon_o \chi_e \mathbf{E} = \varepsilon_o \left(1 + \chi_e\right) \mathbf{E} \tag{2.2}$$

Now, if we define $\varepsilon_r = (1 + \chi e)$, then

$$\mathbf{D} = \varepsilon_o \varepsilon_r \mathbf{E} = \varepsilon \mathbf{E} \tag{2.3}$$

where ε is the permittivity of the material and εr is the relative permittivity of the material, that is, the dielectric constant. Equations (2.2) and (2.3) indicate that the dielectric constant of a material is a measure of its propensity to create dipole moments in reaction to the presence of an electric field. Dielectric constant or relative permittivity (in practice, the two terms are used interchangeably) is an important parameter for dielectrics. Considered slightly differently, it is a macroscopic measure of a material's response, at the atomic level, to an electric field. Dielectric constant is also a materials permittivity normalized to the permittivity of free space:

$$\varepsilon_r = \frac{\varepsilon}{\varepsilon_0} \tag{2.4}$$

Most dielectrics encountered in electronic packaging are isotropic, or their anisotropic properties are small enough that they are ignored. That is, the dielectric constant is essentially or actually the same in all three axes. However, some materials are moderately or strongly anisotropic in dielectric constants [2–4]. Some materials are anisotropic in their "natural" composition. For instance, anisotropy in ceramics is due to their crystal structure. Other "artificial" materials are anisotropic due to their mechanical or chemical composition. Printed circuit board (PCB) materials, for instance, are anisotropic due to the presence of reinforcing weaves of fiberglass and other materials. The dielectric anisotropy means that the value of a dielectric constant depends on the direction of the electric field. For these materials, the susceptibility is a tensor quantity. The dipole moment density is given by

$$\mathbf{P} = \varepsilon_0 \overline{\chi_e} \mathbf{E} \tag{2.5}$$

In this case, the dipole moments that are generated depend on the direction of the electric field. The susceptibility must then be represented by a tensor matrix as follows:

$$\begin{bmatrix} P_x \\ P_y \\ P_z \end{bmatrix} = \varepsilon_o \begin{bmatrix} \chi_{11} & \chi_{12} & \chi_{13} \\ \chi_{21} & \chi_{22} & \chi_{23} \\ \chi_{31} & \chi_{32} & \chi_{33} \end{bmatrix} \begin{bmatrix} E_x \\ E_y \\ E_z \end{bmatrix} \tag{2.6}$$

The result is that the dielectric constant is also a tensor and it is given by

$$\overline{\varepsilon} = \varepsilon_o \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{12} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{13} & \varepsilon_{23} & \varepsilon_{33} \end{bmatrix} \tag{2.7}$$

However, for most dielectrics encountered in microwave and millimeter-wave applications, the off-main-axis elements of the dielectric constant matrix are zero, resulting in

$$\overline{\varepsilon} = \varepsilon_o \begin{bmatrix} \varepsilon_{\text{para}} & 0 & 0 \\ 0 & \varepsilon_{\text{para}} & 0 \\ 0 & 0 & \varepsilon_{\text{perp}} \end{bmatrix} \tag{2.8}$$

where:

$\varepsilon_{\text{para}} = p_{11} = \varepsilon_{22}$ = parallel dielectric parameters (parallel relative to the material sample)

$\varepsilon_{\text{perp}} = \varepsilon_{33}$ = perpendicular dielectric parameter (perpendicular relative to the material sample)

The parallel directed and perpendicular directed relative permittivity are defined in Figure 2.5. Note that the x-directed and y-directed permittivity are equal to each other and are referred to as the parallel dielectric parameter since the vector is directed parallel to the larger dimensions of the substrate. The

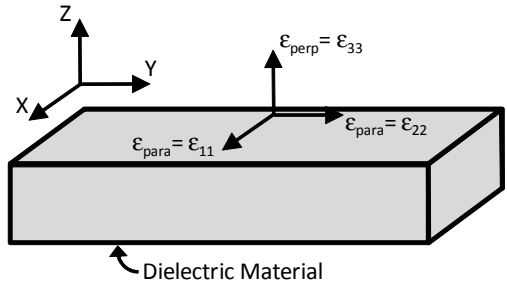


Figure 2.5 An anisotropic dielectric material such as a PCB has a dielectric constant that is the same in the x and y directions but differs in the z direction. (From [5]. Reprinted with permission.)

z-directed permittivity is perpendicular to the substrate and so it is called the perpendicular dielectric parameter.

It is possible to develop a representation of the amount of dielectric anisotropy through a normalized ratio that is given as a percentage and defined as

$$\Delta A_{\varepsilon} = 100 \frac{2\left|\varepsilon_{para} - \varepsilon_{perp}\right|}{\varepsilon_{para} + \varepsilon_{perp}} \quad [\%] \tag{2.9}$$

The anisotropy of several dielectric materials was reported by Dankov [5] and is shown in Table 2.1. Most of these materials are commonly used microwave PCB materials and some exhibit significant anisotropy. The anisotropy varies from 1.0% to 24.6%.

A material is homogeneous if it has the same property throughout the material in a particular direction. Therefore, a material can be locally isotropic, but inhomogeneous. Good-quality microwave dielectrics are homogeneous.

2.1.2 Loss Tangent

The loss tangent was defined in Section 1.1.3 and is given by (1.23). For most practical applications of microwave and millimeter-wave packaging, the loss tangent is considered isotropic. However, a dielectric loss tangent can be anisotropic and is handled in the same way as the dielectric constant so that there

Table 2.1
Measured Data for Several Microwave PCB Materials

Substrate Material	ε_{para}	ε_{perp}	ΔA_{ε} (%)	Using IPC TM-650 2.5.5.5 at 10 GHz
Rogers RO4003	3.67	3.38	8.2	3.38
Arlon 25N	3.57	3.37	5.8	3.38
Isola 680	3.71	3.32	11.1	3.38
Taconic RF-35	3.90	3.45	12.2	3.50
Neltec NH9338	4.02	3.14	24.6	3.38
GE Getec R54	3.91	3.50	11.1	3.90*
Rogers RO3003	3.00	2.97	1.0	3.00
Rogers RO3203	3.18	2.96	7.2	3.02
Neltec NH9300	3.42	2.82	19.2	3.00
Arlon DiClad880	2.32	2.15	7.6	2.17
Rogers RO4003	3.66	3.37	8.3	3.38
Neltec NH9338	4.02	3.14	24.6	3.38
Rogers TMM 10i	11.04	10.35	6.5	9.80

From [5]. Reprinted with permission.
* Measured by split-post cavity.

exists $\tan\delta_{para}$ and $\tan\delta_{perp}$, where $\tan\delta_{para}$ is the loss tangent in the direction parallel to the large dimension of the substrate and $\tan\delta_{perp}$ is directed perpendicular to the substrate as shown in Figure 2.5.

The dividing line between a dielectric and a conductor is the amount of loss the material has in the presence of an electromagnetic field. Good dielectrics have very low conductivity. Good conductors have high conductivity.

2.1.3 Measurement of Dielectric Constants and Loss Tangents

Many methods have been developed to measure dielectric constants and loss tangents [6, 7]. In addition, some industry standards have been developed such as the IPC TM-650 2.5.5.5C. This is a stripline-based test method to measure permittivity and loss tangent at X-band frequencies. However, this method is primarily intended for ensuring quality control during the manufacture of electronic substrates. ASTM D3380-10 is a standard for the measurement of the dielectric constants and loss tangents of polymer-based microwave circuit materials [8].

Dielectric materials measurement methods are either broadband or narrowband based on resonance measurements. Examples of broadband methods are free-space and transmission line techniques. Examples of resonant methods are ring resonators and waveguide cavity resonators.

2.1.3.1 Ring Resonator Method

The ring resonator method [9, 10] uses a transmission line arranged as a ring with input and output capacitive coupling. The resonant frequency of the ring gives the dielectric constant, and the Q of the resonance yields the loss tangent. Figure 2.6(a) shows a sketch of a ring resonator. Note that there are CPW-to-microstrip probe transitions at Port 1 and Port 2. These transitions allow for ground-signal-ground (GSG) probes to be used at a probe station for ease and

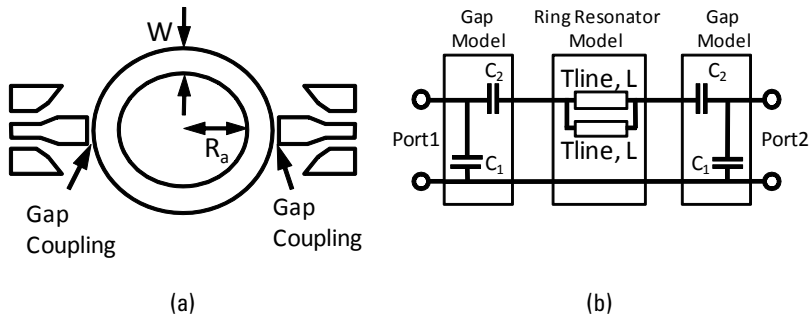


Figure 2.6 Ring resonator: (a) The ring metal pattern has a line width of W, inner radius of Ra, and test signals injected at Port 1 and Port 2. (b) The equivalent circuit models the gap as capacitors C_1 and C_2 and two transmission lines of length L. (*After:* [9].)

accuracy of testing. Note also that the input and output transmission lines do not connect directly to the ring resonator, but instead there is a physical gap in the metal pattern. This allows for loss coupling to the resonator to minimize the loading that occurs from the 50Ω input and output circuits.

The test sample can be modeled electrically as shown in Figure 2.6(b). The input gap is represented by a pair of capacitors. Capacitor C_1 is due the fringing capacitance off the end of the input and output transmission lines. Capacitor C_2 models the capacitance from the input and output lines to the ring resonator. The ring resonator can be modeled using various methods such as using two transmission lines [11] or using an electromagnetic simulator. For the two transmission line method, which involves larger diameter resonators, the curvature can be ignored. Thus, the resonator is analyzed as two transmission lines that are connected at the coupling point to the input and output lines. Because Port 1 and Port 2 are in line with each other, the length of each line modeling the ring is give by $L = \pi R_m$, where R_m is the mean radius of the line. Because the two transmission lines are symmetrically terminated, the resonance will occur when the length of the line is at multiples of a half wavelength, or

$$\frac{n\lambda}{2} = \pi R_m \tag{2.10}$$

where:

λ = the wavelength of the microstrip line mode
R_m = mean radius of the line = $R_a + W/2$
n = the resonance number of the nth resonance

Recognizing that

$$\lambda = \frac{c}{f\sqrt{\varepsilon_{reff}}} \tag{2.11}$$

where ε_{reff} is the effective dielectric constant of the transmission line and $c = 3 \times 10^8$ m/s, which is the speed of light in free space.

We can combine (2.10) with (2.11) to solve for the resonant frequency of the ring resonator:

$$f_n = \frac{nc}{2\pi\left(R_a + \frac{W}{2}\right)\sqrt{\varepsilon_{eff}(f)}} \tag{2.12}$$

Because a microstrip is dispersive, the effective dielectric constant will not be the same at each resonant frequency. Therefore, the effective dielectric constant is shown as being a function of frequency. Once the resonator substrate is measured and the frequency of the resonances is determined, we can solve for the effective dielectric constant by rearranging (2.12):

$$\varepsilon_{reff}(f,n)=\frac{nc}{2\pi\left(R_a+\frac{W}{2}\right)f_n} \tag{2.13}$$

which tells us that the frequency-dependent effective dielectric constant is a function of the resonance number, dimensions of the ring, and resonance frequency. Because the goal is to determine the dielectric constant of the substrate, it is necessary to relate the effective dielectric constant to the dielectric constant of the substrate. Kirschning and Jansen [12] developed an analytic expression for the effective dielectric constant as a function of microstrip line physical dimensions and the dielectric constant:

$$\varepsilon_{reff}(f)=\varepsilon_r-\frac{\varepsilon_r-\varepsilon_{reff}(f=0)}{1+P(f)} \tag{2.14}$$

where:

$$P(f)=P_1P_2\left[0.1844+P_3P_4\right)10fh]^{1.5763}$$

$$P_1=0.27488+\left[0.6315+\frac{0.525}{\left(1+0.157fh\right)^{20}}\right]u-0.065683e^{(-8.7513u)}$$

$$P_2=0.33622\left[1-e^{(-0.03442\varepsilon_r)}\right]$$

$$P_3=0.0363e^{-4.6u}\left[1-e^{-(fh/3.87)^{4.97}}\right]$$

$$P_4=1+2.75\left[1-e^{-(\varepsilon_r/15.916)^8}\right]$$

where:

u = W/h

W = microstrip line width

h = dielectric substrate thickness

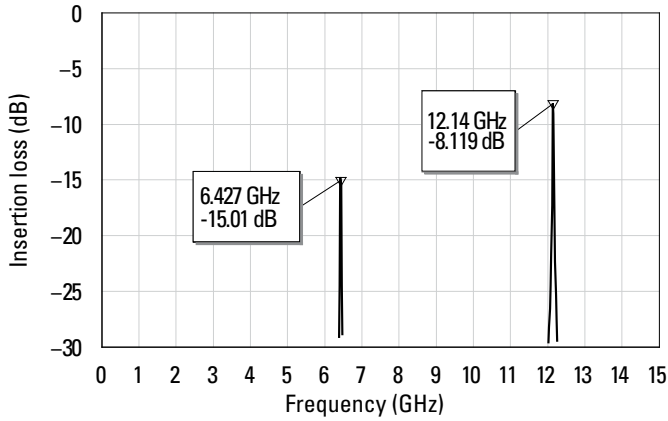
$\varepsilon_{reff}(f = 0)$ = effective dielectric constant at zero frequency

In (2.14) $P(f)$ is the so-called "filling factor," which accounts for the fact that the microstrip line has the dielectric effects of the substrate material and the air region above it. The air region produces microstrip dispersion effects, which cause the effective dielectric constant to vary as a function of frequency. The effective dielectric constant at zero frequency can be determined using the equation from Schneider [13], which is based on conformal mapping and a curve fit:

$$\varepsilon_{reff}(f=0)=\frac{\varepsilon_r+1}{2}+\frac{\varepsilon_r-1}{2}\left(1+\frac{10h}{w}\right)^{-1/2} \tag{2.15}$$

Figure 2.7(a) shows the measured result from a ring resonator that was fabricated using thick film on alumina ceramic. The actual circuit is shown in Figure 2.7(b). As the resonant frequency increases, the ring resonator method becomes less attractive since it is difficult to fabricate small ring resonators and

(a)



(b)

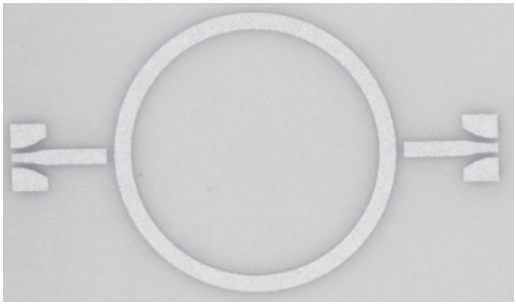


Figure 2.7 Ring resonator (a) measured data, and (b) photo of the fabricated ring resonator. (Ceramic substrates courtesy of CMS Circuit Solutions, Inc., Murrieta, CA.)

the losses due to radiation and conductor loss become more difficult to estimate. Therefore, other techniques are used that rely on cavity resonance methods, as discussed next.

2.1.3.2 Cavity Resonance Method

Resonant cavity methods are an accurate technique for determining dielectric material parameters. A method of split waveguides using cutoff and non-cutoff modes has been developed [14–17]. Figure 2.8 shows a photo of a cavity resonator test circuit. The dielectric sample is placed between the two circular resonator halves. Probes (not shown in the figure) enter each resonator so that the resonant characteristics can be measured. A few important keys to using this method is the ability to lightly couple into the cavities to maintain high loaded Q and the ability to distinguish the desired resonant mode for the other unwanted modes. Through bench testing, it was found that coupling into the resonator can be achieved using a coaxial line with a center conductor formed into a loop.

One benefit of this method is that it is normally nondestructive to the substrate sample. In other words, full-size dielectric substrates can be used in the test. This is helpful since the substrate sample can then be used in circuit fabrication allowing tight tolerances to be maintained on the dielectric constant of the substrates used in manufacturing. For circuits such as filters, which often use transmission line resonators, fabrication with substrates with tight control

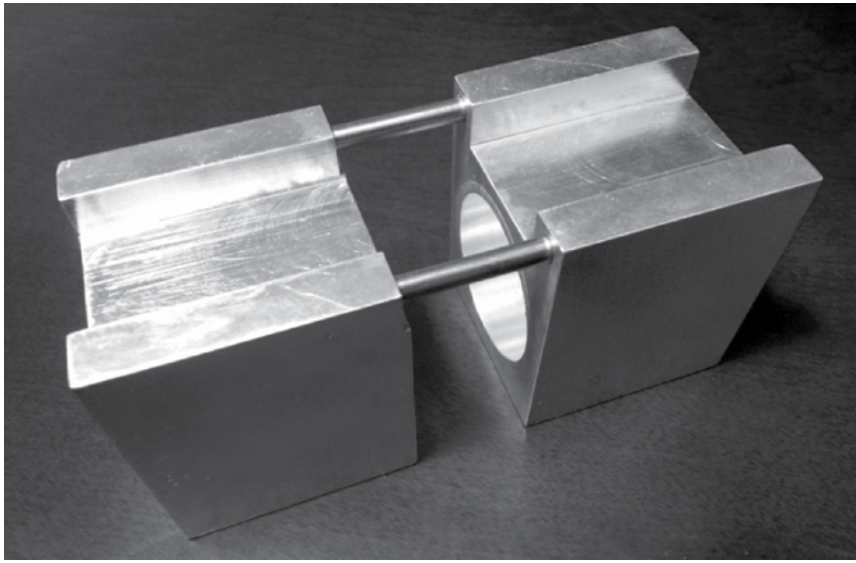


Figure 2.8 A split resonator was fabricated using machined brass and silver plate to measure the dielectric constants and loss tangents of dielectric materials.

over the dielectric constant can be an important advantage. Another benefit of this method is that it does not require costly preparation of the sample. Normally, substrate samples can be directly inserted into the fixture.

As with the other resonance methods, this method uses the measured resonant frequency to determine the dielectric constant and the quality factor of the resonance to determine the dielectric loss of the dielectric sample.

2.1.3.3 Filled Waveguide Method

At millimeter-wave frequencies, it is often desirable to perform measurements using a waveguide since it has a low insertion loss. The dielectric properties of materials can be measured by filling a waveguide with the material and measuring the reflected and transmitted waves [18, 19]. This method relies on the fact that a wave propagating in a waveguide will reflect and transmit energy in a very predictable fashion, which is determined by the dielectric constant and loss tangent of the material. Figure 2.9 illustrates the waveguide with the dielectric sample inserted. Note that the dielectric is not able to perfectly fill the waveguide due to machining tolerances and the fact that the sample must be slightly smaller than the waveguide so that it can be inserted. The sample is smaller than the waveguide in width by $2\Delta X$ and by ΔY.

Since the wave propagating in the waveguide will experience reflections and transmissions, equations for both are needed. The transmitted signal through the dielectric sample is given by

$$|S21| = \frac{1}{\dfrac{\left[1 - \mathrm{Re}^{(-2\alpha L}\right]^2}{(1-R)^2\, e^{(-2\alpha L)}} + \dfrac{4R}{(1-R)^2}\sin^2 \beta L} \tag{2.16}$$

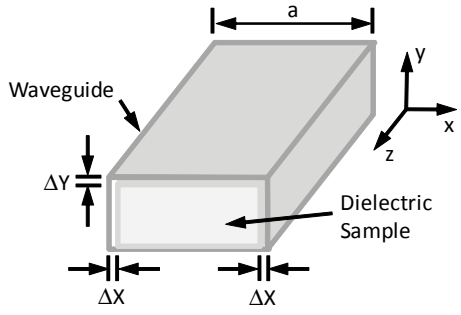


Figure 2.9 A waveguide can be filled with a dielectric material and the reflection coefficient can be measured to determine the dielectric constant and loss tangent.

The reflected signal at the interface of the dielectric sample is give by

$$|S11| = \frac{\dfrac{R\left[1 - e^{(-2\alpha L)}\right]^2}{(1-R)^2 e^{(-2\alpha L)}} + \dfrac{4R}{(1-R)^2}\sin^2 \beta L}{\dfrac{\left[1 - \mathrm{Re}^{(-2\alpha L}\right]^2}{(1-R)^2 e^{(-2\alpha L)}} + \dfrac{4R}{(1-R)^2}\sin^2 \beta L} \tag{2.17}$$

where:

$$\alpha = \frac{\pi}{\lambda_o}\tan\delta \frac{\varepsilon_r}{\sqrt{\varepsilon_r - \left(\dfrac{\lambda_o}{2a}\right)^2}}$$

$$\beta = \frac{\pi}{\lambda_o}\sqrt{\varepsilon_r - \left(\frac{\lambda_o}{2a}\right)^2}$$

$$R = \left[\frac{\sqrt{\varepsilon_r - \left(\dfrac{\lambda_o}{2a}\right)^2} - \sqrt{1 - \left(\dfrac{\lambda_o}{2a}\right)^2}}{\sqrt{\varepsilon_r - \left(\dfrac{\lambda_o}{2\alpha}\right)^2} + \sqrt{1 - \left(\dfrac{\lambda_o}{2\alpha}\right)^2}}\right]^2$$

λ_0 = free-space wavelength = c/f

$\beta = 2\pi/\lambda_0$

ε_r = dielectric constant of the dielectric sample

$\tan\delta$ = loss tangent of the dielectric sample

a = waveguide width

L = length of the dielectric sample.

There are two possible procedures for implementing this method. The first method varies the frequency and the second method varies the length of the sample. Examination of (2.16) and (2.17) shows that they are a function of both β and L. Therefore, the frequency (since $\beta = 2\pi f/c$, where f = frequency and c = speed of light) of the measurement can be swept for a fixed value of sample length. Alternatively, the frequency can be held constant and several samples of various lengths can be prepared. Because high-quality frequency generators are available, it is often more practical to vary the frequency rather than to prepare numerous sample lengths.

Implementing this method is fairly straightforward. The waveguide test system is calibrated without the dielectric sample. The dielectric sample

is inserted into the waveguide and measured. The measured standing-wave (transmission wave or reflected) patterns as a function of frequency are gathered. Next, the insertion loss and/or return loss are simulated using (2.16) and (2.17). The dielectric constant and loss tangent are varied in the simulation (using a root searching tool or error minimization routine) until the simulation matches the measured data to a specified accuracy.

A source of error in this approach is air graphs between the dielectric sample and the waveguide walls. This gap will reduce the predicted dielectric constant and loss tangent. From Figure 2.9, it can be seen that the sample can have an air gap of ΔX at each side wall and ΔY at the top wall (it is assumed that gravity will pull the sample to the bottom of the waveguide). The effect of an air gap on the measured propagation constant is shown in Figure 2.10. Note that the error due to gaps at the side wall are minimal. In fact, for a gap as high as about 0.5 mm (0.25 mm per side wall), the error in propagation constant is less than 0.425%. Keep in mind that this is for WR-10, which is 2.54 mm × 1.27 mm. This is expected because the electric field at the side walls is minimal so that gaps in that region will have minimal effect. However, this is not the case for gaps at the top of the waveguide. For gaps as small as 0.127 mm, the error in propagation constant is nearly 4%. However, it is possible to account for this error and correct for it.

2.1.3.4 Transmission Line Measurements

When designing electronic packaging, it is very useful to know the insertion loss of the transmission line that is being used. This is due to the fact that loss budgets and gain/loss distributions are normally an important part of the design procedure. Therefore, designers need to know the insertion loss of the transmission lines per unit length.

A very simple and straightforward method for determining the insertion loss of a transmission line is based on measurements of several identical transmission lines with various lengths. After the insertion loss of each line length is known, the difference in insertion loss between each line is divided by the difference in length between each line:

$$\text{Line Loss}(\text{dB}/\text{mm}) = \frac{\text{Insertion Loss}_{i} - \text{Insertion Loss}_{i-1}}{\text{Line Lenght}_{i} - \text{Line Length}_{i-1}} \qquad (2.18)$$

This method was implemented for measuring microstrip lines on alumina ceramic substrates using a thick-film process. Figure 2.11 shows an image of the transmission lines. The measured insertion loss was 0.24 dB/cm at 10 GHz.

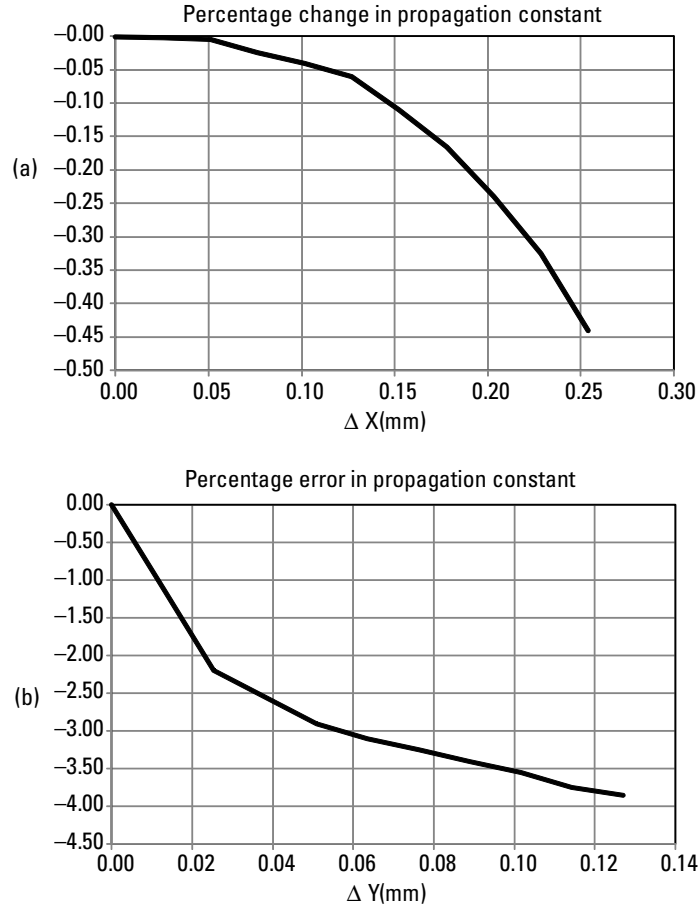


Figure 2.10 The results of an HFSS study show that gaps between the dielectric sample and the waveguide add error to the measurement of dielectric constant for a WR-10 waveguide with a = 2.54 mm and b = 1.27 mm at 95 GHz. (© 1995 IEEE. Reprinted with permission. From: [18].)

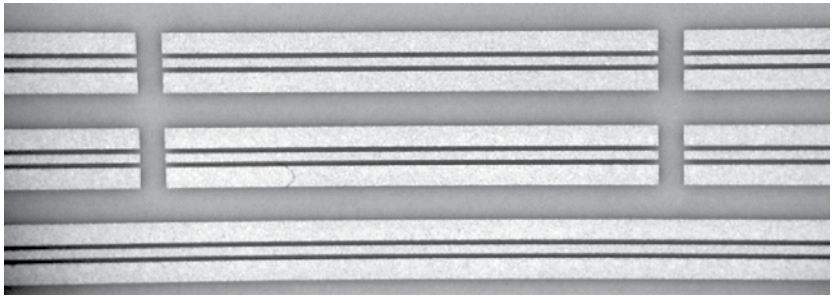


Figure 2.11 Various lengths of microstrip lines were fabricated on 0.381-mm-thick 92% alumina substrates. (Ceramic substrates courtesy of CMS Circuit Solutions, Inc., Murrieta, CA.)

2.1.3.5 Other Methods

Other methods have been used to measured dielectric constants and loss tangents. For instance, free-space methods [20–22] involve placing a material sample between two antennas. By measuring the insertion loss and reflection characteristics, we can determine the dielectric material properties. Another method uses resonant patches on circuit boards to determine dielectric material properties [23–25].

2.1.4 Metal Electrical Conductivity

Metallic materials have free electrons, which give rise to an electric current in the presence of an electric field. For microwave and millimeter-wave packaging, the concerns include the normal low-frequency issues and an additional concern: the skin depth effect (discussed in Chapter 1) increases the transmission line loss.

The losses at zero frequency, or direct current (DC) losses, are a function of the metal's electrical resistivity. For an ideal metal, the DC resistance is just its resistivity multiplied by the length of the metal divided by its cross-sectional area, or

$$R = \rho \frac{L}{A} \tag{2.19}$$

where:

ρ = resistivity of the conductor in units (ohm • meter)
L = length of the conductor
A = cross-sectional area of the conductor.

For many packaging technologies, the resistivity of a circuit is given in ohms per square (often written as ohm/□). The concept of ohm/square is illustrated in Figure 2.12(a), which gives a top-down view of a rectangular conductor of length L and width W. One square is a conductor that has equal length and width. Dividing the total length of the metal trace by its width yields the number of squares:

$$\text{Number of Squares} = \frac{\text{L}}{\text{W}} \tag{2.20}$$

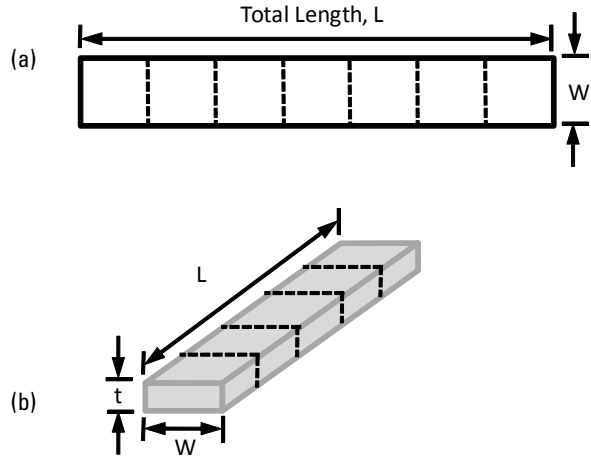


Figure 2.12 For many applications including electronic packaging, it is common to speak of ohms per square in describing the DC loss of a conductor trace as shown (a) in a top-down view of a trace and (b) in an isometric view of a trace of thickness t.

$$\text{Total DC Resistance} = \text{Number of Squares} \;\; \text{Ohms Per Square} = \left(\frac{\text{L}}{\text{W}}\right)\left(\frac{\text{Ohms}}{\text{Square}}\right) \tag{2.21}$$

The ohms/square of a conductor trace can be thought of as the resistivity normalized to the thickness of the metal conductor. This means that it is the responsibility of the packaging manufacturer who quotes metal losses in terms of ohms per square to tightly control the resistivity and thickness of its conductors to maintain the specified ohms per square DC loss. Equating (2.19) and (2.21),

$$\rho\frac{L}{A} = \frac{L}{W}\frac{\text{Ohms}}{\text{Square}} \tag{2.22}$$

Rearranging and recognizing that A = line width × line thickness, we can show that

$$\frac{\text{Ohms}}{\text{Square}} = \frac{\rho}{t} \tag{2.23}$$

Since the ohms per square is the resistivity normalized by the conductor thickness, it provides a useful method for calculating loss. The reason is that, in

practice, it is much easier to count squares and perform a simple multiplication to determine loss. For ceramics, the resistances of metal conductors range from 2 to 20 milliohms/square.

2.2 Mechanical Parameters

The main mechanical parameters of concern in packaging at microwave and millimeter-wave frequencies are thermal conductivity, thermal expansion, Young's modulus stress, strain, and sheer. Thermal conductivity is a concern for electronic packaging at any frequency, but is especially a concern for higher frequencies due to the significant thermal density of some high-power amplifiers. Thermal expansion is also a concern since it is very common for packages to be required to withstand temperature variations from –40° to +150°C in use and as high as +240°C during solder reflow. Young's modulus, stress, strain, and sheer are also important for the reliability and structural integrity of the packaging.

2.2.1 Thermal Conductivity

The thermal conductivity of a material is a measure of its ability to transmit heat. The transfer of energy can occur from electrical carriers such as electrons or holes, lattice waves often referred to as phonons, and electromagnetic waves such as infrared radiation and other methods. For most packaging materials, the total thermal conductivity is given by

$$TC_T = TC_e + TC_p + TC_{EM} \tag{2.24}$$

where:

TC_T = total thermal conductivity
TC_e = thermal conductivity due to electron transport
TC_p = thermal conductivity due to phonon transport
TC_{EM} = thermal conductivity due to electromagnetic wave propagation.

For metals, thermal conductivity is due primarily to electronic processes from free electrons, which is to say, $TC_e > TC_p + TC_{EM}$. In addition, metals are good thermal and electrical conductors since the mechanism of transport in both cases is free electrons. Thermal conductivity due to electron transport is reduced in materials due to electron-phonon interactions and impurities. For dielectrics, thermal conductivity is due primarily to phonon conduction, which is to say, $TC_p > TC_e + TC_{EM}$.

Because electrical conductivity and thermal conductivity in metals result from free electrons, it is interesting to plot thermal conductivity versus electrical conductivity for various metals as shown in Figure 2.13. Note how the different metal types fall roughly along a straight line. The Wiedemann-Franz law states that the ratio of thermal conductivity due to electron processes to electrical conductivity is proportional to temperature and is the same for all metals according to

$$\frac{TC}{\sigma} = LT \tag{2.25}$$

where:

TC = thermal conductivity
σ = electrical conductivity
L = Lorenz number = 2.45×10^{-8} (WΩ/K2)
T = temperature.

In the plot of Figure 2.13, the straight line is just (2.25) solved for thermal conductivity TC and plotted as a function of electrical conductivity. It is clear

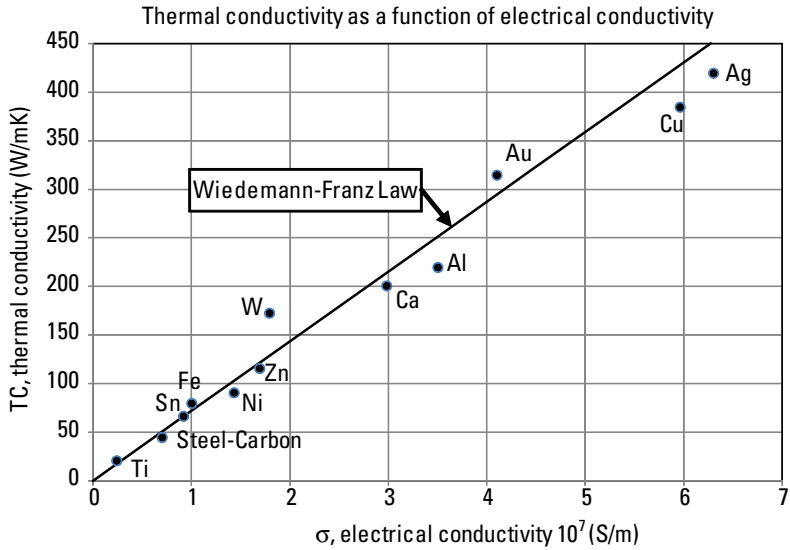


Figure 2.13 The thermal conductivity plotted as a function of electrical conductivity for several different metals along with the ideal Wiedemann-Franz law straight line.

from the figure that the Lorenz number is not exactly the same for all metals, which is why the metals plotted in the figure do not lie in a perfectly straight line. However, for the metals plotted, they do agree with the theory fairly well.

The thermal conductivity of a material is affected in several ways. For instance, at high temperature, thermal conductivity is reduced in most materials. The fact that thermal conductivity varies as a function of temperature must be taken into account in the package design. In addition, for some materials, such as HTCC and LTCC ceramics, the thermal conductivity varies depending on the impurities and additives used by the manufacturer. The thermal conductivity of several materials is shown in Table 2.2.

2.2.2 Thermal Expansion

The thermal expansion of a material is the change in its volume as its temperature varies. The reason that this is of particular importance in electronic packaging is that the majority of packages use several materials that are rigidly or semirigidly attached to each other. Each material has its own expansion rate, and differences in expansion rate will introduce stress as the materials deform at different rates as a result of temperature variations.

Most materials have an expansion rate that is not constant as a function of temperature. Therefore, not only is the material expanding as a function of temperature, the rate of expansion changes as temperature varies.

Table 2.2
Thermal Conductivity and Thermal Expansion of Various Materials Used in Electronic Packaging at Microwave and Millimeter-Wave Frequencies

Material	Thermal Conductivity (W/mK)	Thermal Expansion (ppm/C)
Diamond	1,000–2,000	1.1
Silicon (Si)	150	3.8
Silver (Ag)	429	19.8
Copper (Cu)	380	16.5
Gold (Au)	318	14.2
Aluminum (Al)	240	22
Tin (Sn)	67	22
Silicon carbide (SiC)	310	3.8
Indium phosphide (InP)	65	4.3
Gallium arsenide (GaAs)	55	5.9
Alumina (Al_2O_3)	25	5.4
LTCC	2-4	5.8
Aluminum nitride (AlN)	150	3.5

As an example of the effects of thermal expansion, consider the case of an alumina substrate solder attached to a copper metal base. The coefficient of thermal expansion (CTE) of alumina, from Table 2.2, is 5.4 and the CTE of copper is 22. Figure 2.14 illustrates the effect as temperature rises.

2.2.3 Stress and Strain

When forces act on a material, the material reacts by distributing the force internally. Stress is a measure of the internal forces. The internal force can be assumed to be uniform and the average stress is given by

$$\sigma = \frac{F}{A} \tag{2.26}$$

where F is the positive force acting to elongate the material and A is the area over which the force is applied.

The strain on a material is a measure of the deformation experienced due to external forces. The deformation is normalized to the initial dimensions of the material; thus, the strain is given by

$$\varepsilon = \frac{\Delta L}{L_o} \tag{2.27}$$

where ΔL is the positive force acting to elongate the material and L_0 is the area over which the force is applied.

2.2.4 Young's Modulus

Young's modulus is a measure of the stiffness of a material. It is often supplied in material datasheets and is an extremely important parameter for developing electronic packages. It is defined as

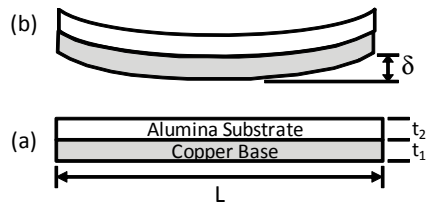


Figure 2.14 Rigidly attached materials with different CTEs will experience deformation (a) at low temperature, t_1, and at (b) higher temperature, t_2.

$$E = \frac{\text{Tensile Stress}}{\text{Stensile Strain}} = \frac{\sigma}{\varepsilon} = \frac{F/A}{\Delta L/L_o} = \frac{FL_o}{A\Delta L} \tag{2.28}$$

Young's modulus can be thought of as the resistance of a material to deformation in the direction of forces applied to it. From (2.28) it can be seen that Young's modulus increases as the amount of deformation, ΔL, decreases. Figure 2.15 illustrates the force F being applied over an area that is the X dimension multiplied by the Y dimension.

As an example, a material measurement was performed in order to determine its Young's modulus. Figure 2.16 shows the results. In the low-strain region of the curve, the stress is proportional to the strain, and the slope of the curve is Young's modulus. From the curve, we can see that as the stress is increased the material enters a nonlinear region and departs from the linear

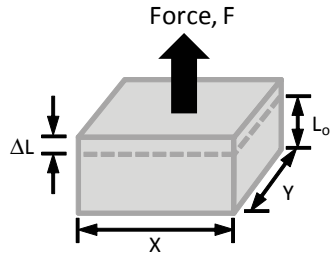


Figure 2.15 Young's modulus is the amount of deformation due to a force over an area.

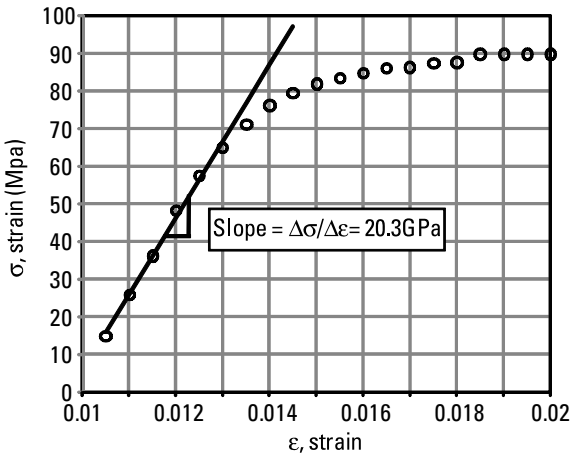


Figure 2.16 Example plot showing the stress and strain of a material and the curve fit in the linear region to extract Young's modulus as 20.3 GPa.

region. The non linear region is often referred to as the "plastic" region. The nonlinear performance of the material is due to the atoms being rearranged and moved to new equilibrium positions. In this region the molecular structure is changing. Some materials do not enter a plastic region, but instead fracture so they are referred to as brittle. Materials that do exhibit a plastic flow region are referred to as ductile.

Stress-strain test specifications and experimental procedures can be found in the American Society for Testing and Materials (ASTM) manuals. Specifically, for metals, use ASTM Test E8, which provides information on testing the strength of ductile materials under uniaxial tensile stresses. For testing plastics, use ASTM D638, which provides information on testing tensile properties to control and specify both reinforced and unreinforced plastic materials. For testing composite materials, use ASTM D3039, which provides information for the testing of in-plane tensile properties of polymer matrix composite materials reinforced by high-modulus fibers.

Questions

1. Prior to which point in the product development process should detailed material properties be determined? What is the impact to the cost of product development if proper material parameters are not determined prior to the completion of the engineering development?
2. Name four of the important material parameters that should be determined prior to product development.
3. What are the three possible physical mechanisms that will generate polarization in a dielectric material and an electric dipole moment?
4. Explain the difference between ε_{para} and ε_{perp} for the dielectric constant tensor.
5. Calculate the effective dielectric constant from ring resonator measurements for resonant frequencies of 5.91, 11.72, and 17.38 GHz for a ring diameter of 6.1 mm and a line width of 0.381 mm. Be sure to calculate the effective dielectric constant at each of the resonant frequencies.
6. The ring resonator from the previous example was fabricated on a substrate that is 0.381 mm thick. Using the effective dielectric constant values calculated from the previous example, calculate the dielectric constant of the substrate.
7. Plot the reflection coefficient as a function of frequency from 80 to 100 GHz for a filled rectangular waveguide material test, assuming the dielectric constant of the sample is 8.5, the loss tangent is 0.003, the

waveguide type is WR-10 with interior dimensions of $a = 2.54$ mm and $b = 1.27$ mm, and the length of the dielectric sample is 1 mm.

8. What is the total resistance of a metal trace that is 4 mm long and 0.05 mm wide if the resistivity of the conductor is 0.005 ohm/square?
9. What is the resistance of a metal trace that is 2 mm long, 0.0254 mm wide, and 0.005 mm thick with a conductivity of 5.8×10^7 (s/m)?
10. In three or four sentences, give a top-level explanation about what thermal expansion is. What happens when two materials with different thermal expansion rates are rigidly attached to each other?
11. What is the difference between a brittle and a ductile material? Give your explanation in terms of Young's modulus and plastic flow.

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3

Ceramic Packaging

Ceramic packaging is of particular benefit to microwave and millimeter-wave products. While it is true that high-performance laminates have been used up to millimeter-wave frequencies for decades, until recently, the vast majority of microwave and certainly millimeter-wave products were fabricated in ceramics. Ceramics are useful in rf products for several reasons:

1. Ceramics are inherently stable due to their very high Young's modulus.
2. It is easy to wire bond to metallized ceramics, allowing for the creation of microwave hybrids.
3. Low-loss ceramics such as alumina and quartz allow for low insertion loss lines.
4. Tight line resolution to 2.5 um (thin film) allowing tight line impedance control.
5. Narrow line widths to 12.5 um (thin film) allowing high-impedance lines.
6. Brazing metals to ceramic is a standard process that allows for the fabrication of hermetic modules.
7. The high thermal conductivity of ceramics allows integration of high-power amplifiers.
8. Blind and buried vias are standard process in cofired ceramics, allowing for high densities.
9. The use of microelectronics on ceramics is highly reliable in extreme temperature environments.

With these benefits, it is no wonder that ceramics were the standard solution for so many years. In Chapter 4, we will discuss laminate circuit boards and how they are now being used in many microwave and millimeter-wave products. This chapter focuses on the types of ceramic processes available.

Although it is true that ceramic packaging is a mature technology choice, the variety of material and processing solutions for it continues to grow. The workhorse processes for ceramics have been thin-film, thick-film, and high-temperature cofired ceramics (HTCC). Thin-film ceramics use metal sputtering on ceramic and etching to achieve the desired metal pattern. Thick-film ceramic metal patterns are placed using a screen printing process. HTCC is realized by printing metal patterns on unfired ceramic tape, stacking them, and then sintering the ceramic at very high temperatures to create a homogenous (except for the internal metal patterns and vias) ceramic. These processing methods, their variations, and other methods are discussed in this chapter.

3.1 History of Ceramics

In the late 19th century, ceramics were machined from soapstone or talc block. The shaped pieces were fired at approximately 98°C to a hard ceramic. The resulting ceramic material was used to produce gas burners in the later 19th century. The burners were used in gas lights for streets and houses and for acetylene lights for automobiles, bicycles, and miners. Using this process, fairly intricate features could be machined into the talc block that would remain during the firing process.

Prior to World War I, Germany was a dominant supplier of porcelain ceramic. However, during World War I, the British naval blockade of the North Sea shut off supplies for chemical and scientific porcelain. At the time, Adolph Coors was president of the Herold China and Pottery Company which was supplying oven-safe cookware. To address the need created by the war, they began producing porcelain. The company was renamed the Coors Porcelain Company at the annual shareholder meeting in 1920.

In parallel with this, the American Lava Corporation developed ceramics for various applications. According to their 1939 company bulletin, they were producing products for burners, pilot lights, nozzles, parts for the chemical industry, parts for electronic vacuum tubes, and thread guides for cotton, silk, and rayon machinery. In fact, they published material datasheets and design guidelines in that same issue of their company bulletin.[1]

1. Special thanks to Adtech Ceramics Company in Chattanooga, Tennessee, and Dr. Bill Minehan for information on the historical development of ceramics technology.

3.2 Thin-Film Ceramics

Thin-film sputtering has been used for many years. Thomas Edison received a patent for a sputtering apparatus in 1902. Edison said that "The value of my process for coating of phonographic-records resides in the fact that the deposited film is so minutely thin as to be accurately deposited upon all portions of the record, so that an absolute accurate matrix or mold can be secured" [1]. However, crude the method may be considered today, his process worked and was applied to solve a very practical application.

Thin-film methods have improved significantly since the days of Edison. Modern thin-film ceramic is fabricated by depositing layers of material and then chemically etching away the undesired areas. The base material is ceramic, usually alumina, although many other materials are used such as quartz, aluminum nitride, beryllium oxide, sapphire, silicon, glass, and ferrites (garnets).

Several methods are used to deposit thin films, but the most common for rf thin-film circuits is sputtering. Figure 3.1 illustrates the thin-film sputtering process. High-energy ion particles are pointed at and hit the target. The target is the material that is to be sputtered on the substrate. The bombardment of ions onto the target causes some atoms of the target to be freed and deposited onto the substrate.

The target can be gold, titanium-tungsten, chromium, nickel, or other metals. Positively charged argon gas ions atoms are excited toward the target. They hit the target with tremendous energy at angle θ. The impact of the argon ion frees atoms from the target and they travel to the ceramic substrate. The rate of sputtering depends on the angle of impact and amount of energy in the argon ion. This process is illustrated in Figure 3.2. The sputtering yield as a function of angle and sputtering yield at a normal angle of incidence ($\theta = 0$) are given by [2]

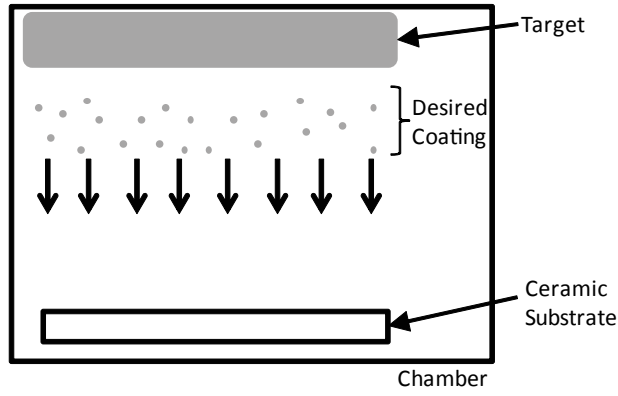


Figure 3.1 Illustration of a chamber for thin-film sputtering.

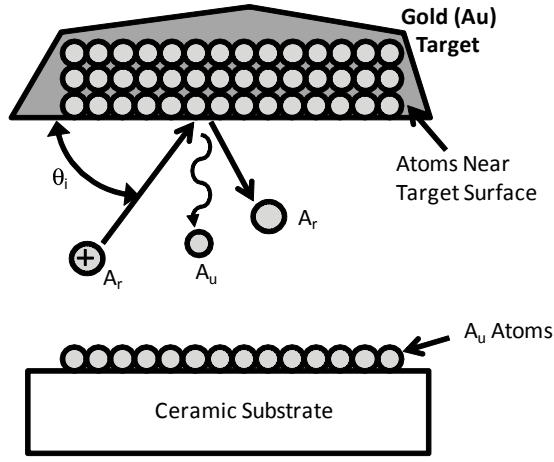


Figure 3.2 Illustration of the sputtering process, which involves argon ions impacting the target to free atoms.

$$Y(\theta)=\frac{Y(0)}{(\cos\theta)^{f}} \tag{3.1}$$

where:

θ = angle of incidence of the ions to the target

$Y(0)$ = yield at a normal incidence

f = exponent dependent on the target and ion mass = 5/3 for most ion/target combinations.

Typically, thin-film circuits are first sputtered with a thin "glue" layer such as titanium-tungsten (WTi). This initial layer provides for the adhesion of subsequent layers. For circuits requiring etched resistors, the glue layer may be nickel chromium (NiCr). The glue layer may only be a few hundred angstroms thick. Often a barrier layer of nickel is added that is a few thousand angstroms thick. Finally, a layer of gold is sputtered and then plated to a thickness of 1 to 4 um depending upon the circuit requirements. Figure 3.3 illustrates the material stack for a typical thin-film substrate.

Sputtering is not the only method for thin-film deposition, but it is widely used. In addition, several different methods of sputtering have been developed. One method uses a DC voltage on the target and electrode. Argon gas enters the chamber and is ionized by the intense electric field between the target and electrode (with the substrate). The electric field is so strong that the ionization creates a cloud between the electrodes. The ions strike the target, which frees

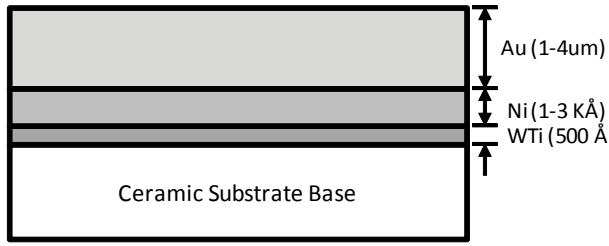


Figure 3.3 Material stack for a typical thin-film substrate.

atoms. The freed atoms migrate to coat the substrate. One drawback to the DC method is that large amounts of charge can be generated, which creates a hazard for workers.

Another sputtering method uses a high-frequency (13.56 MHz is common) voltage in place of the DC voltage. This overcomes the buildup of large amounts of dangerous charge. The rf signal is impedance matched to the rf signal generator to ensure maximum transfer of signal energy. The matching circuit must withstand the high-rf voltages and currents involved. The high temperatures generated during sputtering can create induced stress in some elastic thin films.

Other methods exist such as reactive sputtering, which uses trace amounts of gas such as oxygen. The oxygen can actually exist in the target as inclusions or entrapments for porous targets. As the target is ablated, the inclusions are exposed, which releases the entrapped gas. The gas is actually a contaminant, but also results in the creation of oxides. One problem with the introduction of reactants such as oxygen is that the target will contaminate with the reactant. Needless to say, thin-film deposition techniques have been developed to address these issues.

Most electronic circuits use resistors and their realization in thin films is critical. Several alternatives for the resistor material are available. For instance, it is possible to use NiCr, tantalum nitride (TaN), or nickel vanadium (NiV), though NiV is rarely used as a resistor layer. All of these resistor materials suffer from having their resistance value vary over temperature. Of the three resistor materials, NiCr has been found to the highest temperature stability [3]. The temperature variability can be modeled using

$$R_s = R_o\left[\alpha\left(T - T_o\right) + \beta\left(T - T_o\right)^2\right] \tag{3.2}$$

where:

R_s = sheet resistance at higher temperature T

R_0 = sheet resistance at temperature T_0

α = constant for linear portion of TCR

β = constant for the nonlinear portion of the TCR.

For many resistors, the variability of R_s over temperature is small and linear. Therefore, the nonlinear portion can be ignored, reducing (3.1) to

$$R_s = R_o\alpha\left(T - T_o\right) \tag{3.3}$$

Because the resistive layer of NiCr or TaN covers the whole substrate, it is possible to only realize one resistivity for resistor design. For some products, this can be an important restriction. Very common resistor values are 50 and 100 ohm/square. The realization of large-value resistor values can be difficult. This is due to the fact that large-value resistors can become physically large. To overcome this limitation, large value resistors (>1 kΩ) are often realized using epoxy attach and wire bond resistors.

The chambers used to sputter the material are complex. Figure 3.4 is a photograph of a modern sputtering system. Processes such as the insertion of gases and voltage controls are used to achieve the most efficient and uniform transfer of material from the target. The sputtering machines are used to fabricate circuits for a variety of products including semiconductors, light-emitting

Figure 3.4 Thin-film chamber. (Courtesy of KDF Electronic & Vacuum Services, Inc., Rockleigh, NJ.)

diodes, and flat-panel displays to name just a few. Sputtering systems are part of a larger family of processes referred to as physical vapor deposition (PVD).

Because the targets are the source of material that is deposited onto the thin-film circuit, their purity and maintenance are important. Target materials can be pure metals such as gold or nickel, alloys such as TiW, and nonmetals. Figure 3.5 shows several targets. They are fabricated in a variety of geometries such as rectangular, rings, and circular.

Advanced thin-film processes include the use of linear scanning, velocity profiling, and planetary rotation [4]. This technique overcomes one of the obstacles of uniformity and repeatability in thin-film layer thickness. The method is able to achieve a uniformity of better than +/−1% and a repeatability of better than +/−0.5%. This represents about a 10 improvement over standard processing. Although this method has been used for high-quality optical mirrors, it may find uses for high-tolerance thin-film capacitors for microwave and millimeter-wave filters and other tuned resonant circuits. Figure 3.6 shows the rotating system.

The PVD processes can be used to create a variety of circuits. For microwave and millimeter-wave packaging, thin films processed on ceramics are normally integrated into a multichip module or housing. In addition, thin-film circuits can be used for a variety of circuits. Figure 3.7 shows thin-film circuits for amplifier boards, millimeter-wave hybrid couplers, and DC interconnects.

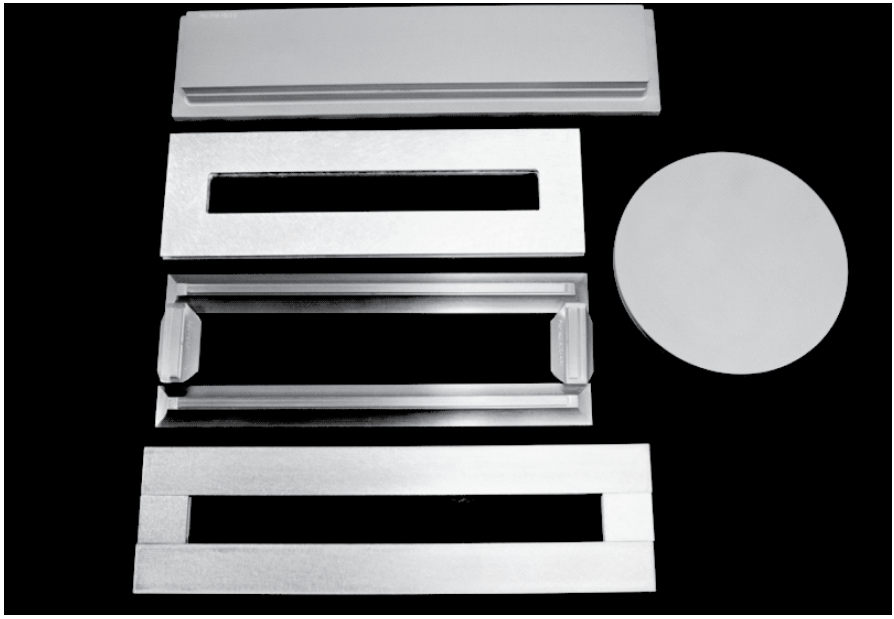


Figure 3.5 Targets used in physical vapor deposition. (Courtesy of KDF Electronic & Vacuum Services, Inc., Rockleigh, NJ.)

Figure 3.6 Thin-film vapor deposition rotating system used to achieve higher uniformity and repeatability in thin-film layers. (Courtesy of KDF Electronic & Vacuum Services, Inc., Rockleigh, NJ.)

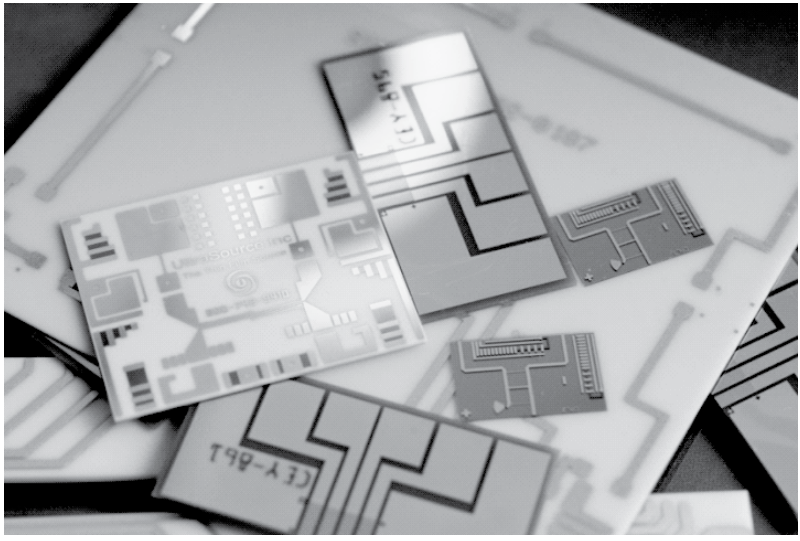


Figure 3.7 Various thin-film circuits. (Courtesy of UltraSource, Inc., Hollis, NH.)

Laconte, Flandre, and Raskin have analyzed the stress and strain in thin-film oxides with completely elastic deformation [5]. They found that because the thin-film layers are so thin compared to the ceramic substrate they are attached to and since the thin-film is able to move in the Z direction, thin-film stress only exists in the X and Y directions as illustrated in Figure 3.8. With the assumption of static equilibrium, the stress can be written as

$$\sigma = \begin{pmatrix} \sigma_X & 0 \\ 0 & \sigma_Y \end{pmatrix} \tag{3.4}$$

Hard materials such as silicon dioxides (SiO_2) and silicon nitride (Si_3O_4) can be assumed to be completely linear elastic and therefore obey Hook's law. The stress and strain are linearly related as

$$\begin{pmatrix} \varepsilon_X \\ \varepsilon_Y \end{pmatrix} = \begin{pmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{pmatrix} \begin{pmatrix} \sigma_X \\ \sigma_Y \end{pmatrix} = H \begin{pmatrix} \sigma_X \\ \sigma_Y \end{pmatrix} \tag{3.5}$$

which tells us that the stress is equal to the elastic matrix times the strain. The elastic matrix consists of two Young's moduli and the Poisson ratio as

$$H = \begin{pmatrix} 1/E & -v/E \\ -v/E & 1/E \end{pmatrix} \tag{3.6}$$

where E represents Young's modulus and v is the Poisson ratio. Therefore, the stress strain relationships can be written as

$$\varepsilon_X = \frac{1}{E}\left(\sigma_X - v\sigma_Y\right) \tag{3.7}$$

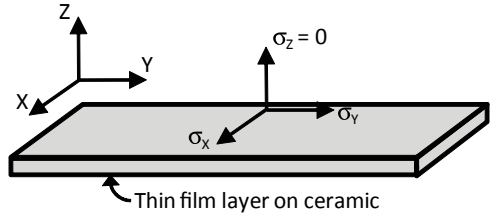


Figure 3.8 Thin-film layer on ceramic exhibit stress only in X and Y directions.

$$\varepsilon_Y = \frac{1}{E}\left(\sigma_Y - v\sigma_X\right) \tag{3.8}$$

For deposited thin films the materials can be considered isotropic so the X and Y components of the stress and strain are equal. Therefore, (3.7) and (3.8) simplify to

$$\sigma = \left(\frac{E}{1-v}\right)\varepsilon \tag{3.9}$$

The thin-film material on the ceramic substrate experiences stress and strain. This is caused by the elevated temperatures used during the deposition process and then subsequent cooling, or by temperature variations during subsequent processing, or by temperature variations in the final application. Whatever the cause of the temperature variation, the strain is

$$\varepsilon(T) = \varepsilon(T_o) + \alpha\Delta T \tag{3.10}$$

where:

$\varepsilon(T_0)$ = the strain at the reference temperature
α = coefficient of thermal expansion
ΔT = temperature change from the reference temperature.

The final step in the thin-film process is plating of the thick top metal, which is normally gold (Au). An electroplating process is commonly used because it can be controlled. The metal thickness that is plated is affected by several parameters including the plating time, electric current density and current efficiency, the presence of additives or impurities in the plating bath, the type of metal being plated, type of plating voltage (DC, pulsed DC, AC, etc.), orientation of the plated part, exposure of the metal (plating in holes), and temperature. The relationship of plating thickness to plating time is given by [6]

$$\frac{T}{t} = \frac{JE_p\alpha_p}{\rho_p}$$

where:

T = thickness of the plating

t = time
J = current density
E_p = electrochemical equivalent
α_p = current efficiency
ρ_p = density of the deposit.

3.3 Advanced Thin-Film Techniques

Thin-film circuit processing is increased in complexity to the point that highly integrated multilayer circuits can be fabricated and highly reliable filled vias can be processed. Figure 3.9 shows filled vias in circuit with spiral inductors. The filled vias allow for low resistance and a low-inductance interconnect to the ground plane under the ceramic. The combination of the fine lines of the spiral inductors and high electrical performance vias allows for the realization of wideband bias circuits and filters.

Thin-film processing now allows for multilayer processing as shown in Figure 3.10. Production processes now exist for three conductor layers and two polyimide layers. The gold conductor layers can be processed to less than 25-um lines and spaces to permit high-density designs. Tantalum-nitride resistive material is also deposited on the first layer to allow realization of resistors and matched terminations.

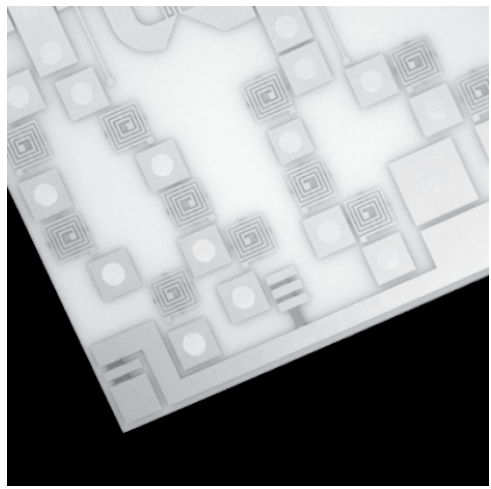
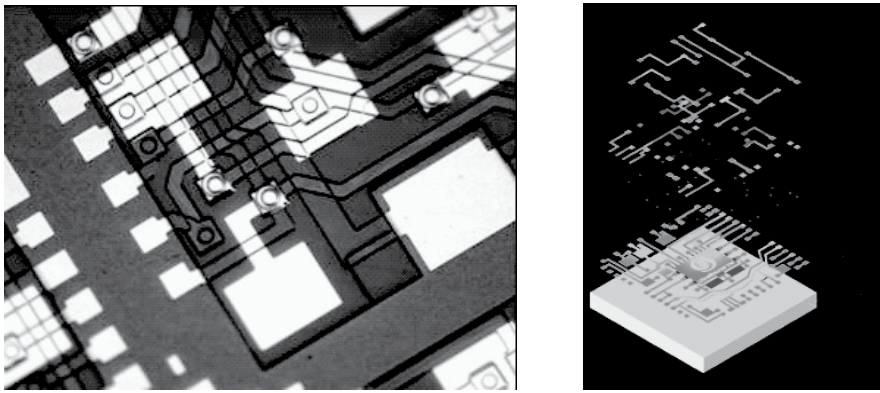


Figure 3.9 Advanced thin-film processing allows for filled vias. (Courtesy of UltraSource, Inc., Hollis, NH.)



(a) (b)

Figure 3.10 Advanced thin-film processes allow for the realization of multilayer thin-film circuits. (Courtesy of UltraSource, Inc., Hollis, NH.)

3.4 Thick-Film Ceramics

Thick-film ceramic starts with a hard ceramic substrate as a base just as with thin films. However, whereas the creation of thin-film ceramics is a deposit-and-etch process, thick-film ceramics are created by an additive process in which each layer is printed and then fired in a furnace. Thick film has several advantages and some drawbacks compared to thin film. The advantages are as follows:

1. The designer is not restricted to one value of ohm/square for resistors.
2. It is possible to have low-cost solid vias (gold, copper, or silver).
3. In high volumes, thick films are lower cost than thin films.
4. Printed metal and dielectric layers can be used to create complex circuits.

Thick film suffers from some drawbacks compared to thin film. Most of the limitations are due to the fact that thick film is printed. Drawbacks include the following:

1. The narrowest printed line is about 75 um, although 125 um is a standard process.
2. An etched thick film can realize lines as narrow as 25 um, but it is more costly.
3. Line width resolution is 25 to 50 um, resulting is more variation in line impedance.

4. The surface roughness of thick films can increase line losses.

The thick-film process consists of 10 main elements. Figure 3.11 illustrates the printing of thick film and the different elements as they exist as part of the fabrication process.

3.4.1 Thick-Film Paste

The paste used to pattern thick-film ceramics can be metal, resistor material, or dielectrics. The metal material is normally gold, although other metals can be used such as copper (Cu), silver (Ag), palladium-silver (AuPd), platinum-palladium-silver (AgPdPd), and platinum-gold (AuPt). The gold thick-film metal is typically 8 to 12 um thick, although etched thick film can be as thin as 1 to 2 um.

Gold is by far the most common thick-film metal used in microwave and millimeter-wave circuits. This is due to the wire bondability of thick-film gold. However, gold is not solderable, so for applications requiring wire bonds and soldered components, it is common to mix the thick-film metallization. In such a case, it is possible to use both gold metal paste and palladium silver paste on the same substrate.

Most conductor pastes contain glass frit, binders, and other organic material. The frit adds in adhesion to the substrate and the organic material burns off during firing. After each layer is printed, it is sent through a furnace running at 700° to 1,000°C depending on the paste being used.

In addition to metals, dielectrics can be printed. Often, dielectrics are printed to permit multiple metal layers. The dielectric functions as an insulator to isolate metal layers so that overlapping metal can be created.

Resistor material is printed to create resistors. Resistor pastes are normally referred to as inks. The design of resistors uses the concept of ohms per square that was introduced in Section 2.1.4. One benefit of a thick film is that multiple resistor ink ohms/square values can be used. This can be a significant benefit

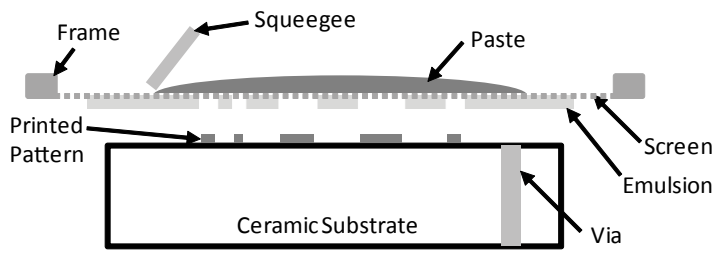


Figure 3.11 Illustration of the thick-film printing process.

for designs requiring very large value resistors and very small value resistors on the substrate. For instance, it would be difficult to realize a 2-Ω and 2-MΩ resistor on the same substrate if only one value of resistor ink was available. However, it is possible to fabricate as many as three to five different resistor ink values per substrate.

The thick-film pastes (or inks) are viscous. Viscosity can be thought of as the "thickness" of the material. Water has a low viscosity and is often referred to as thin. As a very practical example, the viscosity of thick-film pastes is somewhere between the viscosity of the condiment ketchup and tomato paste. The rheology of thick film is another important characteristic. Rheology refers to how a material flows in plastic deformation.

3.4.2 Squeegee

The squeegee presses the paste onto the substrate through the mesh and emulsion of the screen. Highly trained and skilled technicians or automatic machines move the squeegee across the screen. If too much pressure is applied to the screen, it can be damaged. If too little pressure is used, then the paste material will not pass through the screen and deposit on the substrate.

3.4.3 Frame

The frame supports the screen and emulsion. The frame is normally fabricated from aluminum to provide the mechanical stability required for precision screen printing. The frame will have the correct dimensions and mounting feature required by the screen printing machine.

3.4.4 Screen and Mesh

The screen material is normally fabricated from stainless steel or polyester. An important parameter for the screen is the mesh opening. This is because the mesh opening affects the line resolution that can be printed and the maximum particle size that will fit through the opening. If the line width to be printed is too small, the opening in the emulsion may be covered by the wire diameter of the mesh. In this case, the material will not be able to get past the mesh to flow into the opening in the emulsion. This results in a failure due to the missing conductor line. If the opening is too small, the particles in the paste may not fit through the mesh.

The printing process causes the mesh to stretch. Over time, the screen will stretch enough that it will need to be replaced so that printing accuracies can be maintained. After each printing, the screens must be carefully cleaned and stored for future use.

3.4.5 Emulsion

The emulsion determines the pattern that will be printed onto the substrate. In addition, the emulsion thickness determines the thickness of the paste being printed.

3.4.6 Desired Metal Pattern

The main point of printing thick films is to achieve a pattern of metal, dielectrics, and resistors. Achieving the desired metal pattern may require from 5 to 50 or more print and fire cycles, depending on the number of layers used.

3.4.7 Ceramic Substrate

The substrates are normally sent out for laser machining as the first step in the thick-film process. The laser machining process places holes and other features in the ceramic. The holes are later filled or barrel coated during thick-film processing. By far, alumina (Al_2O_3) is the preferred material for thick-film substrates, although beryllium oxide (BeO) and aluminum nitride (AlN) are also used.

The laser processing of holes in the ceramic is accomplished using very high-power CO_2 lasers that bore holes through the ceramic. Proper processing results in clean holes without microcracks in the ceramic. The vias will have a slight taper so that the entry point of the via is slightly smaller than the exit point.

3.4.8 Printing Machine

The machine that prints the material can be a completely manual machine or fully automatic. The printing machine must hold and align the ceramic and the frame. Also, the squeegee is part of the printing machine. Manual printing machines can have a very long service life of 20 years or more.

3.4.9 Etching

Etched thick film is an attractive option for applications requiring fine lines and spaces. It allows for the realization of many of the benefits of thin film, but with the flexibility of thick film, such as multiple resistor ink values and lower cost in high-volume production. For etched thick films, the gold conductor is printed and fired as thin as 1 um over an area that is larger than the desired conductor pattern. Then, the substrate is patterned using an etching process very similar to that used for thin-film processing. It is possible to realize line widths as small as 25 um.

3.4.10 Postprocessing

After the thick-film processing is completed, some applications require postprocessing such as resistor trimming and metal brazing.

When resistors are designed, they are sized to be 80% of the final desired value. Then, the resistors are laser trimmed to the final desired value. Some thick-film products require metal features such as ring frames. Metal features are often brazed using AgSn or other solder.

3.5 Thermally Enhanced Thick-Film Processes

Thick-film ceramic substrates have been enhanced using methods such as direct bond copper (DBC) and high thermal conductivity filled vias. The DBC methods vary depending on the manufacturer. Figure 3.12 shows a cross section of an alumina substrate with directly bonded copper. The copper forms a strong bond to the alumina and an excellent thermal path. Other methods for realizing thick copper include thick copper plate over printed thick-film silver [7]. The benefit of this method is that the other thick-film capabilities such as printed gold, printed resistors, and plugged and plated vias can be included in the circuit.

3.6 High-Temperature Cofired Ceramic (HTCC)

HTCC is extremely common and is used in a variety of applications such as crystal packages, microprocessor packages, transmit/receive modules, and optical sensors. In high volumes, it can be very low cost. However, the tooling costs required for high-volume production can be significant.

The vast majority of HTCC is fabricated with either black or white alumina. However, some applications have been found for HTCC aluminum nitride (AlN) due to its high thermal conductivity compared to alumina.

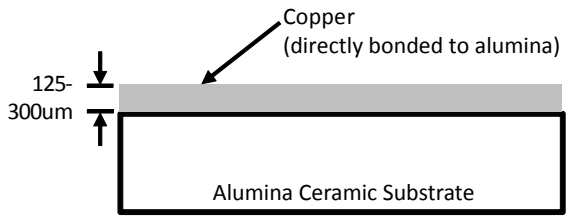


Figure 3.12 The DBC method uses a layer of copper foil, which is bonded at high temperature (1,000°C) to form a strong bond to the alumina substrate.

An important defining characteristic of HTCC is that it is fired at very high temperature. HTCC alumina is typically fired at approximately 1,600°C and HTCC AlN is fired at approximately 2,000°C. Another important characteristic about HTCC is that it is fabricated by firing multiple layers of material to create a homogenous substrate.

Another characteristic of HTCC is that is must use refractory metals for the metals that are fired with the ceramic. This is due to the high temperatures involved. Noble metals such as gold, silver, and copper would not survive the firing temperature. For instance, the melting temperature for gold is 1,064°C, which is well below the processing temperatures of HTCC. The refractory metals that are commonly used include tungsten (W) and molybdenum (Mo). These metals have melting temperatures of 4,320° and 2,620°C, respectively. Although the resistivity of these refractory metals is high compared to gold or silver, it is common practice to plate the surface metallization such as transmission lines to improve the insertion.

A simplified process flow for the manufacturing of HTCC is illustrated in Figure 3.13. The first step of the process is the mixing of the ceramic slurry. The tape casting pushes the slurry through a tool to create tape layers. The tape layers are punched with holes according to the requirements of each particular design. The holes are filled with metal and each conductor layer is printed. The layers are stacked and dried prior to furnace firing. The final step is postprocessing such as plating, brazing, machining, and grinding.

3.6.1 Slurry

The first step in the process is the preparation of the slurry. The slurry is the liquid material that is used to create the dielectric layers. The slurry contains

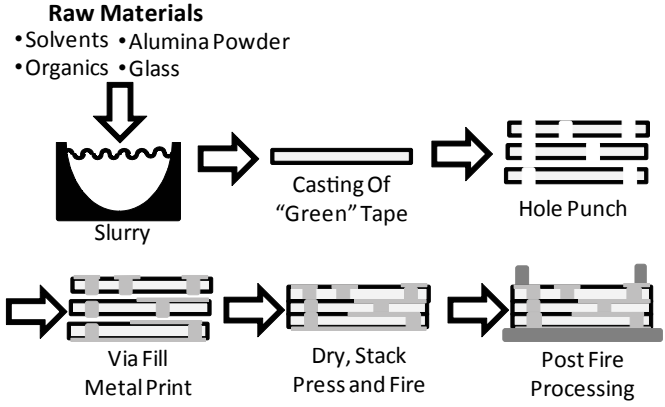


Figure 3.13 Illustration of the processing steps to realize cofired packaging.

ceramic, glass, binding material, and solvents. Some fabricators formulate and manufacture their own slurry, whereas others purchase green tape. The slurry is created by mixing alumina that has been milled and ground into a powder with specified particle sizes. The solvents and binders serve to create the slurry which is transferred into the tape casting machine.

The alumina powder used to create the slurry must have a very small particle size. Ideally, the particles will be 0.1 to 1.0 um. The particle size is normally analyzed and statistics are gathered on the distribution of the average particle size. The goal is to have a small standard deviation for the particle size so that the material is as uniform as possible.

Before the slurry is sent to tape casting, it is mixed to create a uniform distribution of the materials so that the microstructures can be controlled.

3.6.2 Tape Casting

The slurry is pushed past a tape casting stage to create "green" alumina tape layers. The goal is to have green tape layers that are dense and have as uniform a distribution of material as possible (tight packing). The layers are not actually green in color. Once dried, the green tape layers have the flexibility and feel of vinyl seat material. The thickness of the tape cast layers typically varies from 0.1 to 0.5 mm, though it is very common for tape layers to be between 0.125 and 0.25 mm. Tape casting machines can be quite large and complex. Figure 3.14 shows an image of a ceramic tape casting machine. In the figure, the slurry enters the tape caster at the far end of the machine. At the near end of the figure, the tape is rolled.

3.6.3 Punching

The next step in the process is the punching of vias. Because each layer can have distinct via sizes and locations, each tape layer must be separately punched. At low volumes numerically controlled (NC) punch machines are used to create the via holes since the costs of programming and running NC machines are lower than costs associated with a commitment to production tooling. Also, it usually makes sense for an engineering or preproduction product, which may experience design changes, to be fabricated using NC punch machines. High-volume production uses tools to generate the holes in the green tape.

The preferred diameter of the via is determined by the thickness of the layer. HTCC fabricators speak of the ratio of the via diameter to the thickness of the substrate. Most manufacturers prefer a ratio of about 1:1. For instance, a 0.25-mm-thick substrate will have 0.25-mm vias.

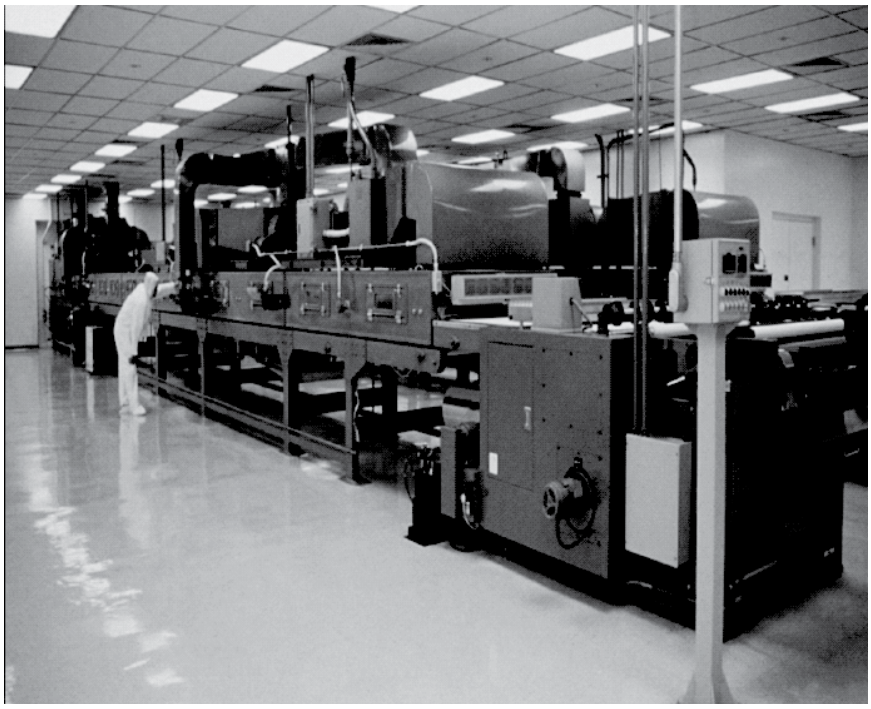


Figure 3.14 Tape casting machine. (Courtesy of Adtech Ceramics Company, Chattanooga, TN.)

3.6.4 Via Filling and Conductor Printing

The vias are filled and each layer is printed with its metal pattern. The via filling and printing process is essentially the same as for thick films except that the metal is not fired prior to stacking.

3.6.5 Stacking, Pressing, and Cofiring

The layers are then stacked, pressed, and cofired to create the electronic package. The alignment between layers is important for maintaining an electrical connection. If one layer is misaligned to the next, the vias that are indented for electrical connection may not line up properly. To overcome this difficulty, the fabricators require the use of via catch pads placed over the vias. This ensures that the via will make contact with the metal printed on the layer and that the vias between layers will connect.

The layers are then pressed together and fired. The firing profile is guarded by most fabricators as proprietary information. Typical firing temperatures are about 1,600°C. During the firing process, the solvents are burned away and the material shrinks in volume by about 20%. Fabricators have developed

methods to control and predistort the metal patterns so that the final product achieves the required conductor locations and dimensions. Figure 3.15 shows an image inside a furnace with HTCC being fired during the 24-hour process.

3.6.6 Postprocessing

After the firing process is complete, the HTCC ceramic is processed in ways similar to those used for thick-film ceramic. The HTCC ceramic can be plated, lapped, ultrasonically machined, and brazed with metal such as seal rings, leads, and heat sinks. Brazing is normally with silver copper or gold tin eutectics. Figure 3.16 shows several finished HTCC parts with gold plating and brazed metal bases.

3.7 Low-Temperature Cofired Ceramic (LTCC)

LTCC is characterized primarily by the fact that it is fired at much lower temperatures than HTCC, which allows noble metals to be used. Therefore, it is common to see LTCC packages with a gold- and silver-based metal system. Some fabricators have developed methods to fabricate LTCC with copper metal systems. Another characteristic is that some suppliers have ceramic formulations that are lower loss than HTCC alumina. In addition, since the firing temperature is low enough, it is possible to include surface and buried resistors.

Figure 3.15 Furnace with HTCC ceramic elevated to 1,600°C. (Courtesy of Adtech Ceramics Company, Chattanooga, TN.)

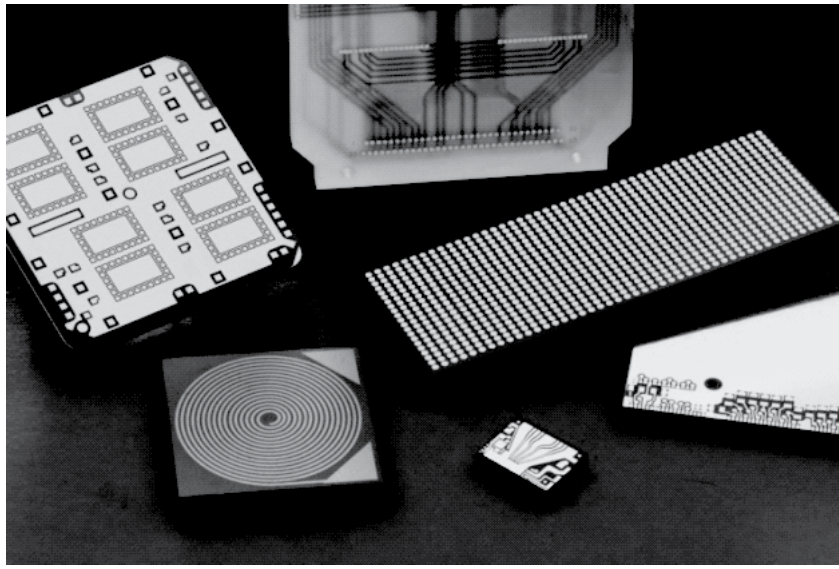


Figure 3.16 Several HTCC finished parts. (Courtesy of Adtech Ceramics Company, Chattanooga, TN.)

This can be a significant benefit since buried resistors allow for the realization of buried circuits such as power dividers, couplers, and attenuators.

The fabrication process is very similar to that used for HTCC. However, most fabricators purchase the LTCC "green" tape layers from a small number of suppliers. The green tape layers are punched with holes, filled, and printed with metallization. The layers are then dried, stacked, and fired. The resulting material is then postprocessed using metal brazing, laser or ultrasonic machining, or post-fire printing.

Metal systems for LTCC have improved significantly so that some of the early issues with wire bondability have been substantially addressed. One drawback to LTCC is that it is not as strong mechanically as HTCC ceramic.

The benefit of being able to use noble metals and the low dielectric losses of some LTCC materials have resulted in LTCC being used for applications as high as W-band [8–10].

Questions

1. With the assumption that a thin film is homogenous, show the detailed derivation of (3.9).
2. List six reasons why ceramic materials are useful for electronic packaging at microwave and millimeter-wave frequencies.

3. For a typical thin-film process, what material is the "glue" layer and why is it used?
4. Describe at least two sputtering methods. Be sure to mention their benefits and/or drawbacks.
5. What are the two common thin-film resistances (ohms/square) that are available from most manufacturers?
6. Given that thin-film resistors can have a temperature coefficient for their resistivity that is as high as +/−50 parts per million per degree centigrade, what is the maximum and minimum resistance of a resistor at 230°C if it has a resistance of 50Ω at 23°C.
7. List four advantages and four drawbacks to using thick-film ceramics.
8. What is a thermally enhanced thick-film substrate? How is the thermal performance improved compared to conventional thick films?
9. How is tape casting used in high-temperature thick-film processing?
10. What is the main difference between HTCC and LTCC? What are the differences in the types of metallization that are used for internal metal features? Why is this important for microwave and millimeter-wave packaging?

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4

Laminate Packaging

Laminate circuit board packaging has moved from being useful only for low-frequency applications to being the preferred method for ultralow-cost packaging for many microwave and millimeter-wave applications. This chapter explores the manufacturing process used in creating laminate circuit boards. The most common PCB material is FR-4, however, it has limited application for microwave and millimeter-wave applications due to its high loss tangent. Therefore, high-performance laminates have been developed. Liquid crystal polymers are also used to create microwave circuit boards. Laminate multichip module (MCM-L) methods provide the designer the option to create highly integrated solutions using low-cost PCB techniques. In this chapter, the terms PCB and laminate are used interchangeably.

Printed circuit boards must be able to handle subsequent processing temperatures. For instance, lead-free soldering can require temperatures as high as 260°C. The circuit board must withstand this temperature during repeated reflow cycles without sustaining damage. Common circuit boards have glass transition temperatures, T_g, in the range of 130° to 180°C for FR-4 material. Some higher performance materials, such as modified epoxy and hydrocarbon ceramic laminates, have glass transition temperatures as high as 280°C. The glass transition temperature marks the change in a material from a hard, rigid state into a soft, rubbery state. It is a reversible process so that once the material's temperature is lowered, it returns to its rigid state.

Although T_g is an important parameter for materials, it is often not the most significant parameter for laminate circuit boards. Instead, the decomposition temperature, T_d, is often used as a figure of merit. This is the temperature at which permanent degradation to the material occurs and there is a 5% weight loss in the material. For most laminates, T_d is in the range of 300° to

400°C. Each material has its own characteristics and most laminate datasheets will show both T_g and T_d.

4.1 Laminate Board Fabrication

The laminate circuit board process steps are shown in Figure 4.1. The process starts with delivery of the database to the supplier and continues to final testing and inspection. Although the figure simplifies the process steps, it does capture the major fabrication steps. Each manufacturer has its own variation on the process. For instance, it is common to tailor the process by adding inspection points and additional bake-out steps. Nevertheless, the processes, as outlined, provide an accurate overview.

4.1.1 Database Review and Acceptance

As the first step in the process, the design database must pass an engineering and manufacturing review. The design database consists of the Gerber files, hole drill file, and the fabrication drawing. The Gerber files are specially formatted data files that contain the metal pattern for each layer, via catch pads, solder mask, silk screen, and so forth. The Gerber file format was developed by Joseph Gerber at the Gerber Systems Corporation. The hole drill file is also generated by the design database software and contains the coordinates and tool size (hole drill size) for every hole in the circuit board. The fabrication drawing is also generated by the design program and contains a view of the overall circuit board and its dimensions, any special features, and the fabrication instructions with callouts for the required fabrication specifications to be followed.

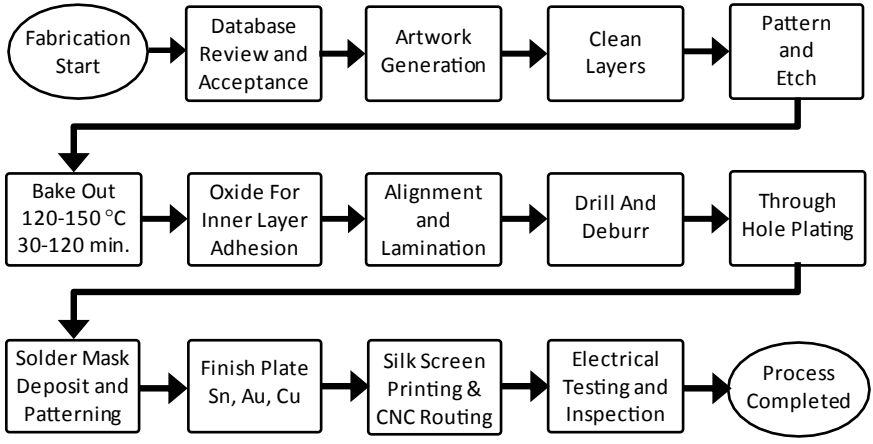

Figure 4.1 Simplified laminate circuit board process flow.

4.1.2 Artwork Generation

In the artwork generation step of the process, the masks that are used in subsequent process steps, such as etching the metal pattern and generating the solder mask, are created. The artwork is generated by dedicated artwork machines that generate transparent film with the desired metal pattern on them.

4.1.3 Clean Layers

The cleaning step removes any material on the layers prior to patterning and etching. Otherwise, surface contaminants on the layers can cause rejects due to improper metal etching. For boards that already are photosensitized, this cleaning operation is not used.

4.1.4 Pattern and Etch

Circuit board fabricators start their fabrication process with prefabricated laminate boards that already have the copper cladding on both sides of the boards. Some circuit boards have photoresist (photosensitized) ready for fabrication. The photoresist is exposed so that the areas where copper is desired have a protective coating of the photoresist material. In the other areas where copper is not desired, the copper is exposed so that the unwanted copper is etched away using an etching technique. This leaves the copper board with the desired metal pattern.

In another method, used for quick prototyping, the undesired material is removed using a computer numerically controlled (CNC) milling machine. In this approach, the boards are mounted on a CNC machine using a vacuum plate. The boards are then machined to remove the undesired metal. This is time consuming, but during development stages, it reduces engineering time for new product development.

4.1.5 Bake-Out

Most board processes include several bake-out stages. The purpose is to remove any volatile substances before the next process steps. The bake-out process is conducted at 120° to 150°C for 30 to 120 minutes. Care must be taken during bake-out processes such that prior processes are not damaged. For instance, bake-out at too high a temperature can damage oxide treatments.

4.1.6 Oxide Treatment of Inner Layers for Adhesion

The inner layers of the circuit boards are treated with a black oxide to improve adhesion of the stacked layers. The inner layers with exposed copper are actually submerged in black oxide baths. The black oxide is from the copper oxide

(also called cupric) in the tank. It forms a layer on the surface of the copper that improves the copper adhesion to subsequent lamination with prepreg layers. Mil-F-495E is specification for black oxide use on copper metals and has been used by manufacturers.

4.1.7 Alignment and Lamination

Alignment fixtures ensure that layers are properly aligned during the lamination process. The lamination step is the stacking of laminate core material with prepreg (the adhesion layer). The stack is pressed at high temperatures (340° to 400°C) for as long as 90 minutes. This process causes the prepreg to cure and act as a glue to hold the stack together. After the material is laminated it is ready for drilling. Figure 4.2 shows the stack up of a typical laminate circuit board. The core material layers and prepreg material layers are shown. Under lamination, the prepreg layers melt and form around the metal features.

4.1.8 Drill and Deburr

After the lamination process is complete, the circuit boards are drilled and deburred. The drilling process uses the coordinates and the tool information from the hole drill file. The tool information instructs the drill machine about which diameter tool to use for creating the hole, and the hole locations instruct the machine about where to place the holes. The deburr process removes any extra material at the drill locations and prepares it for through-hole plating.

4.1.9 Through-Hole Plating

Electroless copper plating is used to plate the through holes. The holes are typically barrel plated; Figure 4.3 shows an image of a barrel coated via in a laminate circuit board. Notice that the metal only covers the inside radius of the hole, leaving the hole intact. This is important since some components use the

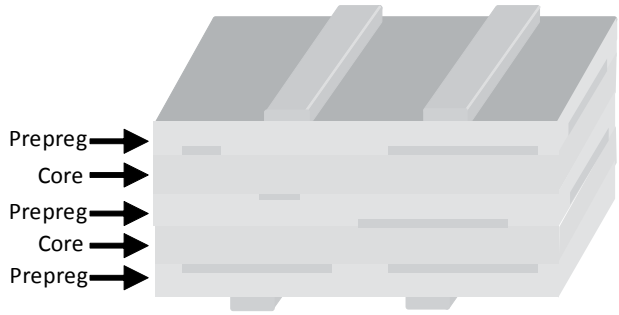

Figure 4.2 Cross section of the material stack for a typical laminate circuit board.

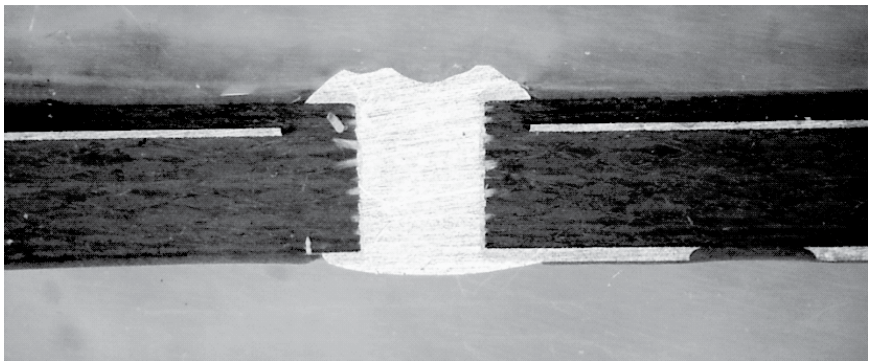

Figure 4.3 Barrel coated via filled with solder in a laminate circuit board. (Courtesy of New-Tek PCB, Inc., Orange, CA.)

through hole for attachment. However, in other applications, the hole needs to be plated shut. This can be accomplished in two different ways. First, the hole can actually be plated shut by the copper plating. This requires significant copper material and is only practical for small-diameter holes. It is very common for the hole to be first barrel coated followed by filling of the via with a conductive epoxy. The via is then pated over the top with copper so that it has a clean copper finish. For some QFN packages with thermal pads, this filled and capped via method is preferred so that solder flow can be controlled to achieve maximum adhesion. This can be critically important since the thermal performance of high-power dissipation QFN packages relies on maximum solder connection from the package thermal pad to the board solder pad with thermal vias.

4.1.10 Solder Mask

Solder masking is an important step because it creates the openings for most of the solder attached components. The solder mask can also be important for opening the proper solder pad sizes for some QFN packages. Achieving a correct solder mask design normally starts at the first stages of the design process when the component libraries are generated. Careful review of all component libraries is a critical step in the design.

4.1.11 Finish Plating

The finish plating covers the exposed copper and improves its reliability. For high-reliability applications, all exposed copper is gold plated with a flash of gold. Most applications require a tin plate of the exposed copper.

4.1.12 Silk Screen and CNC Routing

The silk screen layer is printed onto the substrate. It has the component reference designators, part number, company logo, electrical connection information, and special instructions. This layer is defined by the Gerber files. The next step is CNC routing, which simulates the substrates from the panel in which they were fabricated.

4.1.13 Electrical Testing and Inspection

The circuit board is electrically tested to determine if there are any errors in fabrication. For high-volume circuits, a bed-of-nails test fixture is created so that the testing can be done rapidly for many connection points at once. For low-volume circuits, a flying probe test machine is used. Final inspection confirms compliance with all of the internal and customer-specified requirements. Once the parts have received final inspection approval, they are ready to be shipped to the customer.

4.2 Cost of Laminates

For most laminate circuit boards, the first production cost driver is the material. The larger the circuit board, the more expensive it becomes. Another cost driver is the type of material used. FR-4 material is much lower cost than some high-performance microwave laminates. Also, the cost varies significantly between the available suppliers of microwave laminates. The other cost drivers are:

- *Metal finish:* Boards with a tin finish are much lower cost than boards requiring a gold finish.
- *Minimum line width:* As the line width and gaps decrease, the cost to fabricate the circuit boards increases. This is partly due to the fact that finer line boards will have lower production yields. Also, very fine line boards will require special attention during the etching process.
- *Number of holes:* As the number of holes increases, the cost of the board increases.
- *Blind or buried vias:* If blind or buried vias are required, the cost of the circuit board increases.
- *Smallest hole size:* Hole diameters below about 0.5 mm will increase the cost of the board.

- *Plated slots or special holes:* Some manufacturers offer the fabrication of plated via slots but at an added cost. Also, castellated vias add an extra cost.
- *Board shape:* Generally, a board manufacturer can manufacture almost any board shape. However, boards with internally machined features are expensive.

The approximate cost of a PCB circuit board can be modeled using a closed-form equation. With the assumption that learning occurs as the number of circuit boards increases, the PCB cost can be modeled as follows:

$$\text{PCB cost} = C_0 + M_c N^{-\alpha} A + \left(N_v - 5\right) A C_v + A N^{-\alpha} \sum_{k=1}^{q} P_k \qquad (4.1)$$

where:

C_0 = a constant cost adder containing most of the profit
M_c = material cost per square centimeter (i.e., dollars/cm^2) per board
N = number of circuit boards ordered
α = experience curve exponent = elasticity of cost with respect to output
A = area of the board in square centimeters
N_v = number of vias per square centimeter
C_v = cost per via
P_k = secondary processes cost per square centimeter, per board
k = number of secondary processes

The first term in (4.1) is C_0, which is the cost adder that the manufacturer adds to the order as profit and to account for possible unknowns that may add to the overall cost. In addition, for some orders, the cost adder includes the value based on what the manufacturer perceives the customer is willing to pay. If the customer believes that the manufacturer provides some additional value, such as proximity to their factory, on-time delivery record for a time-sensitive project, or other factors, and if the manufacturer knows this perceived value, then the manufacturer may choose to increase the cost to capture this value.

The second term in the cost model is essentially the cost of the material with the learning curve effects. The material cost, M_c, includes the cost per square centimeter of each layer in the circuit board such as the core layers, prepregs, and mask layers. An important part of the second term in the cost model is the learning curve. As the number of circuit boards, N, increases, the

cost of fabricating each board is reduced. This effect can be modeled using experience curve methods and is captured by the elasticity of cost exponent, α. The cost per unit decreases as the number of units increases for several reasons. In particular, the labor cost per unit is reduced for circuit boards that require more labor steps. As the number of boards increases, the factory floor becomes more efficient due to standardization and methods that are implemented. Also, the cost of equipment used in the manufacturing process can be amortized over a larger number of circuit boards, thereby reducing the cost per board. The majority of the cost of a PCB is due to material costs and the fact that as the number of units increases, the efficiency of the manufacturing process increases so that the experience curve effect reduces the cost per board.

The next term in the cost model includes the cost of drilling vias in the PCB. The production process assumes that a number of vias will be drilled per square centimeter and the cost of any vias over that number must be included in the model. In the model, it is assumed that the base pricing includes five vias per square centimeter. If the via density is over this number, then the cost per board is increased by cost per via.

The last term in the cost model accounts for any added optional processes. For instance, some circuit boards require a gold finish on all metal surfaces. Other designs require the use of fine lines and spaces, which will impact the overall yield. Another example is blind and buried vias, plated holes, and slots. Because the cost of these secondary processes depends on the number of boards and the size of the board, the coefficient in the model includes the number of boards and the board area. The cost secondary processes will be reduced as the number of circuit boards increases due to experience effects. The experience curve exponent reduces the cost as the number of units increases. The last term, therefore, captures the secondary processes and includes the experience curve effects.

4.3 Laminate Circuit Board Tolerances

Although laminates offer a significant cost benefit, a few of the features of these types of materials must be taken into account. For instance, the tolerances for laminate circuit boards are higher compared to ceramic. This is also true for the minimum feature size (line width and gap) that can be achieved. Also, the substrate thickness has higher tolerances. Other things to consider are that some laminates will cold flow, which can be a mechanical concern in some applications.

One of the biggest issues in using laminates and PCB technology at microwave and millimeter-wave frequencies is the manufacturing tolerances that can be achieved. For instance, for standard processed boards, the minimum

line width is 0.18 mm and line width tolerance is +/- 0.05 mm. Compare this to thin-film ceramic boards, which can achieve +/-0.0025 mm, and thick-film ceramic, which can achieve +/-0.025 mm. For some applications this tolerance difference can impact performance. The main contributor of line width and gap tolerances is the thickness of the conductor. Because of the ability of the exposure methods and etching methods, the line width tolerance increases as the thickness of the transmission line metal increases.

As an example, consider the microstrip line in Figure 4.4. Assume that the transmission line is fabricated in thin film, thick film, and laminate and that in all cases the transmission line returned from the fabricator with their line width at its maximum allowed tolerance. If the substrate thickness is fixed at 0.25 mm and the dielectric constant is 9.8, we can compare the impact of line width tolerance on a 50Ω transmission line. The nominal line width is 0.24 mm to achieve 50Ω line impedance. For thin film the line width came in at 0.24 mm + 0.0025 mm = 0.2425 mm. For thick film the line width came in at 0.24 mm + 0.025 mm = 0.265 mm. For laminate the line width came in at 0.24 mm + 0.04 mm = 0.29 mm. The transmission line impedance for each of these cases is shown in Figure 4.5. Note that the line impedance increases as a function of frequency due to dispersion. Also note that the error in transmission line impedance resulting from the error in line width tolerance is about 1.5% for thin film on ceramic, 5.8% for thick film on ceramic, and close to 10% for laminate. This analysis assumes a higher dielectric constant than is normally used for laminates so that a comparison to ceramics can be made. For lower dielectric constants, the error will be less and calculation of it is left as an exercise.

Some fabricators offer specialized metallization processes that can achieve narrower lines and gaps with lower tolerances. These processes tend to require the custom deposition of very thin layers of metallization, which can be expensive.

In addition to line width and gap tolerances, the tolerances on via diameter and associated via catch pads can have an important impact on performance. This is especially true for boards with buried rf signals. The purpose of the via catch pad is to ensure that the via makes contact with the signal line. This is important because the machine that drills the hole in the circuit board that makes the via has some tolerance on its location. Therefore, the annular ring must be

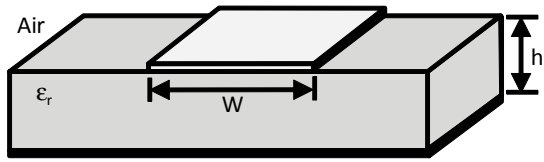

Figure 4.4 Microstrip line with line width *W* and substrate thickness *h*.

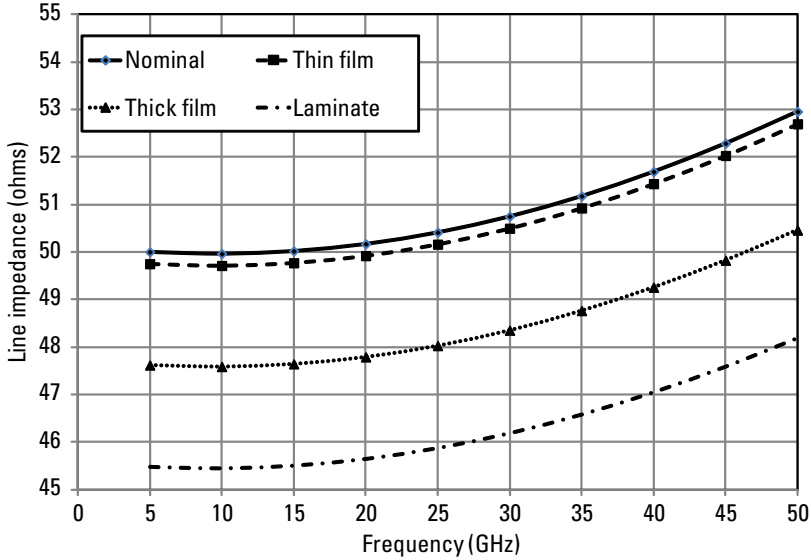

Figure 4.5 Analysis results of line impedance change as a function of frequency assuming the maximum tolerance based line width increase for thin-film ceramic, thick-film ceramic, and laminate circuit board for a 0.254-mm-thick substrate with a dielectric constant of 9.8.

larger than the via. Figure 4.6 illustrates the layout of a catch pad with the signal line entering and the catch pad around the via. The electrical modeling of vias and the via catch pad are covered in Chapter 7.

Another important tolerance is the thickness of the circuit board. Consider a buried stripline as shown in Figure 4.7. The standard board thickness tolerance is +/− 10%. If the circuit board thickness is $B = 0.75$ mm, then the standard tolerance is +/− 0.075 mm. Figure 4.8 shows the curve for stripline

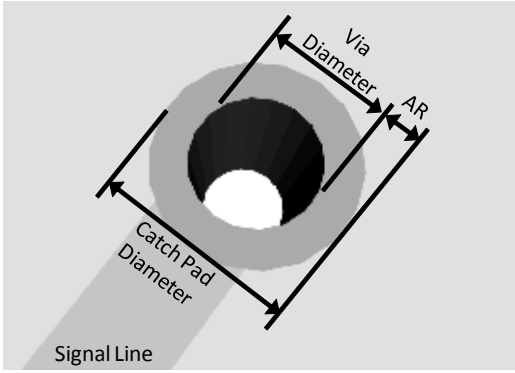

Figure 4.6 The via catch pad is used to ensure that the via makes contact with the signal line.

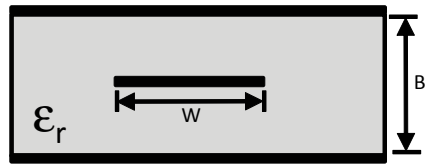

Figure 4.7 Stripline transmission line with line width W and substrate thickness B.

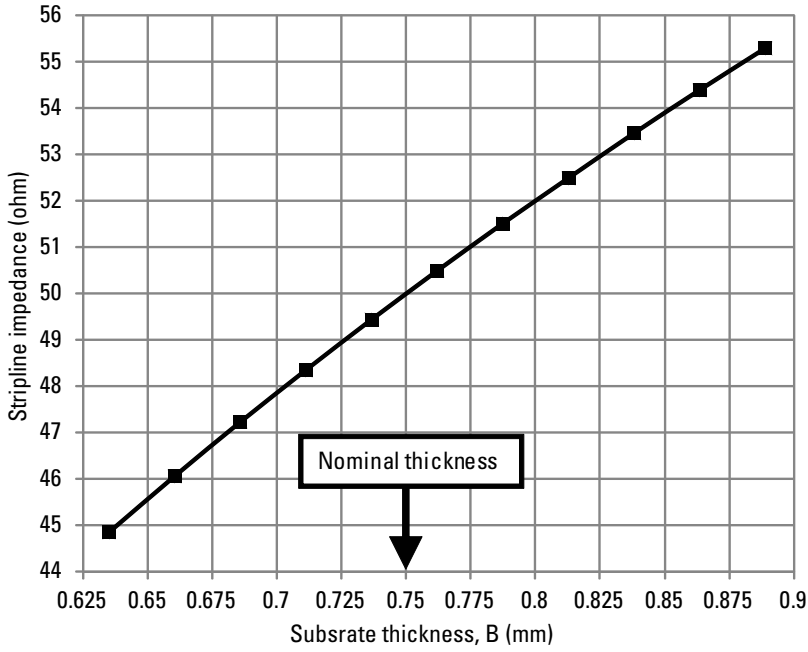

Figure 4.8 Line impedance change for stripline as a function of substrate thickness change.

impedance as a function of substrate thickness. Note from the curve that a +/−10% change in substrate thickness will cause the line impedance to vary from 46.79Ω to 53.01Ω.

4.4 High-Performance Laminate Materials

For application at microwave and millimeter-wave frequencies, FR-4 is not a practical choice as the material for transmission lines. This is because it has a very high dielectric loss tangent, which means that the rf signal energy is absorbed by the FR-4 and dissipated as heat. Therefore, high-quality laminate materials are used that have much lower dielectric losses and also lower dielec-

tric constant. These improved materials can have dielectric losses that are 10 to 50 times lower than FR-4.

As an example of the benefit of using high-quality laminates, consider a stripline transmission line as shown in Figure 4.8 and used in an application at 60 GHz. Because the signal traveling on the stripline is a transverse electromagnetic mode (TEM), the dielectric loss can be modeled as

$$\alpha_d = \frac{\pi}{\lambda} \tan\delta \tag{4.2}$$

where:

α_d = loss due to dielectric loss (Np/m)
λ = wavelength within the material
$\tan\delta$ = loss tangent.

For the case of FR-4 with a dielectric loss tangent of 0.03 and a dielectric constant of constant of 4.7, the dielectric loss at 60 GHz is 3.55 dB/cm. For the case of a high-quality laminate material with $\varepsilon_r = 3.45$ and $\tan\delta = 0.003$, the dielectric loss is 0.305 dB/cm. As can be seen, the dielectric loss of FR-4 is high, which makes its use as a dielectric for transmission lines impractical at 60 GHz. And for most applications, FR-4 is not a viable solution for transmission lines above a few gigahertz. However, FR-4 can still be used to route DC and low-frequency control signals.

Most high-quality microwave laminates that are available in the marketplace use either a glass-reinforced Teflon-based material, ceramic resin-based material, or liquid crystal polymer material. Each of these materials has certain benefits and drawbacks.

4.5 Liquid Crystal Polymer

Liquid crystal polymer (LCP) is a type of partially crystalline polyester. Although its crystal structure is less ordered than that of a regular crystal, it is possible to create ordered structure while remaining in the liquid phase. LCPs are inert, which makes them a candidate for many applications including food processing and industrial and consumer products. One of the benefits of LCP material is that it has very low water absorption rates. This is important for high-reliability applications or for applications that use unprotected integrated circuits that are mounted onto the LCP material. They are halogen free, inher-

ently flame resistant, and can be fabricated to have a low coefficient of thermal expansion.

LCP material has been successfully used in several different formats for microwave and millimeter-wave applications. One format is as an injection-molded electronic package [1–5]. In this process, LCP material is injection molded around a copper frame. The copper frame contains the electrical connections from the outside of the package to the bonding pads for the integrated circuit. These integrated circuit packages are very similar to QFN-style packages except that they have an air cavity. The air cavity allows the rf integrated circuit, which has sensitive circuits on its surface, to have air over it. This results in a minimum effect on the electrical performance of the circuitry on the integrated circuit. This type of packaging using LCP is attractive for applications to 40 GHz and higher.

The other type of application for LCP is as a type of laminated package and module [6]. In this method, the LCP material is fabricated into layers that can be laminated using standard PCB fabrication methods. The manufacturers of this material have developed prepreg material as well as the core materials. This technique has been used to create very complex multilayer circuit boards, including applications requiring conformal electronics [7]. Other applications include multilayer circuit boards with LCP covers that are laminated to circuit board to create a hermetic or near-hermetic solution with interconnects and transitions that perform to 38 GHz [8]. A similar demonstration was achieved in the 13- to 25-GHz range with an LNA package [9]. The versatility of laminate circuit boards has allowed them be used in demonstrations at 60 GHz for very low cost consumer electronics [10]. It allows the inclusion of antennas to create fully integrated solutions.

4.6 Laminate Multichip Modules

Modules have been formed using laminate substrates. The cost benefits are significant when compared to traditional multichip modules that use metal housings or ceramic packages. In fact, the cost benefit offered by laminates has made some millimeter-wave product feasible. These laminate modules are called laminate multichip modules (MCM-Ls).

One method uses commercially available GaAs MMICs on top of a laminate substrate. As part of that development, the insertion loss of several transmission lines was measured. Microstrip lines were shown to have about 0.21 dB/mm of insertion loss at 70 GHz, and the coplanar waveguide (CPW) was shown to have about 0.3 dB/mm of insertion loss at the same frequency. Clearly the motivation for technology development at these frequencies is to take advantage of the 71- to 76-GHz and the 81- to 86-Hz bands for line-of-sight

backhaul communication networks. Figure 4.9 shows an MCM-L. Note that it uses three MMICs to achieve a transmit function with a mixer, low-noise amplifier, and medium-power amplifier. It has microstrip and stripline connections between the MMICs at the input/output. The required bypass capacitors are included in the module [11].

4.7 Conclusions

Laminated circuit boards used to be exclusively utilized at low frequencies. However, the use of high-performance laminate circuit boards has increased significantly. In fact, it has been demonstrated that laminate circuit boards may be the only viable solution for high-volume, low-cost, millimeter-wave-enabled consumer products.

Questions

1. Assume that you are given the task of selecting the materials for a laminate package that must survive postprocessing temperatures of 250°C, must have a dielectric constant in the range of 2.5 to 3.5, and must have a dielectric loss tangent lower than 0.005. Perform an Internet search for possible laminate circuit board materials that have a glass transition temperature higher than your maximum postprocessing temperature.
2. Analyze the impact of line width changes for the same cases shown in Figure 4.4 except assume that the dielectric constant is 3.55, substrate thickness is 0.2 mm, and be sure to use the correct line width to achieve 50Ω in the nominal case and add the tolerances.

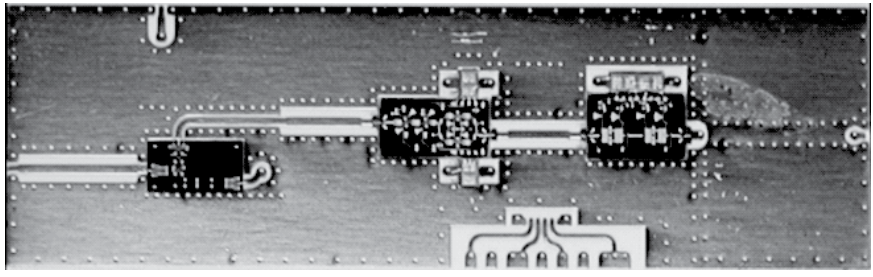

Figure 4.9 Three GaAs MMICs are integrated into a single, low-cost laminate circuit board. (© 2011 IEEE. Reprinted with permission. From: [11].)

3. Perform the same analysis as in Question 2 but instead of microstrip lines, assume that a conductor-backed coplanar waveguide is being used.
4. Calculate the dielectric loss of a microstrip in decibels per centimeter, assuming FR-4 and a high-quality microwave laminate ($\varepsilon_r = 3.45$ and $\tan\delta = 0.03$) are used at the dielectric material and an operating frequency of 60 GHz.
5. Perform the same analysis as in the Question 4 except consider a stripline. Write a paragraph comparing the usefulness of FR-4 for millimeter-wave applications for an rf transmission line.
6. Analyze a 50Ω stripline transmission line and determine if the line impedance sensitivity to laminate substrate thickness changes of +/− 0.05 mm assuming a dielectric constant of 3.55, and a nominal substrate thickness of 0.5 mm.
7. What is liquid crystal polymer and how might it be useful for microwave and millimeter-wave packaging?

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5

First-Level Interconnects

First-level interconnects exist between ICs and packages or a next level assembly. Some examples are wire bonds, ribbon bonds, and flip chip interconnects.

First-level interconnects at microwave and millimeter-wave frequencies are more challenging than for lower frequency or DC applications because interconnect electrical characteristics can have a major impact on the performance of an IC. An example is parasitic effects such as undesired stray capacitance from an interconnect. The parasitics from a wire bond have capacitive or inductive effects that degrade electrical performance. Figure 5.1 shows the insertion loss of a series inductor as a function inductance from 0 to 1 nH at 25 GHz. Note that only about 0.5 nH of inductance is required to create 2 dB of insertion loss. Other concerns from first-level interconnects include undesired signal coupling to surrounding circuits, resonances on the interconnect, and radiation effects that can cause the interconnect to perform as an antenna. For instance, at millimeter-wave frequencies, radiation from wire bonds can result in signal loss and undesired coupling to other circuits. For accurate modeling at these frequencies, additional model fidelity is required and many applications rely on cosimulation of the packaging with the integrated circuits to fully capture radiation and undesired coupling effects. Therefore, proper attention must be paid to their design to avoid problems such as insertion loss and return loss issues.

5.1 Wire Bond Interconnects

Wire bond interconnects are, by far, the preferred first-level interconnect used in electronics. As a result, the installed supplier base for providing wire bond processing is significant. Their widespread use is partly due to their low cost and

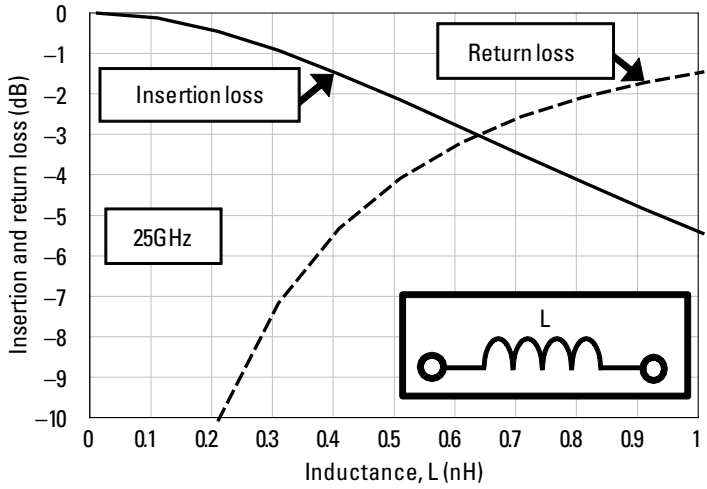


Figure 5.1 Even a small amount of series inductance can have a significant effect on insertion loss and return loss.

robustness. Therefore, designers should have a proper understanding of wire bond interconnects and their electrical modeling and optimization.

5.1.1 Wire Bond Manufacturing

Wire bonds are formed by placing small-diameter wires between the input/output (I/O) pads of an IC (or other component) and the bond pads of a package or next level assembly. For microwave and millimeter-wave ICs, gold wires are the standard. Other materials such as aluminum and copper are used, especially for lower frequency power devices, or high-volume assembly where the cost of gold wire is prohibitive. Figure 5.2 is a photograph of aluminum wires placed using a wedge bond tool.

A wire bond interconnect forms a metallurgical bond between itself and the bond pad on the IC and the next level assembly, such as a thick-film bond pad on a ceramic substrate. Ideally, the wire metal and the bond pad metal are the same material; for example, gold wire bonds on gold IC bond pads and gold bond pads on the next level assembly. However, it is very common for gold wire bonds to be placed on aluminum IC bond pads. The wire bond interconnect can be thought of as a type of microweld between the wire bond and the bonding surface. For very low cost, high-volume applications, copper wire is being used because it has a much lower cost than gold wire.

Wire bonds can be connected to a bond pad by using ultrasonic bonding, thermocompression bonding, and thermosonic bonding. Ultrasonic bonding uses pressure and ultrasonic vibrations from a bonding tool to create the bond

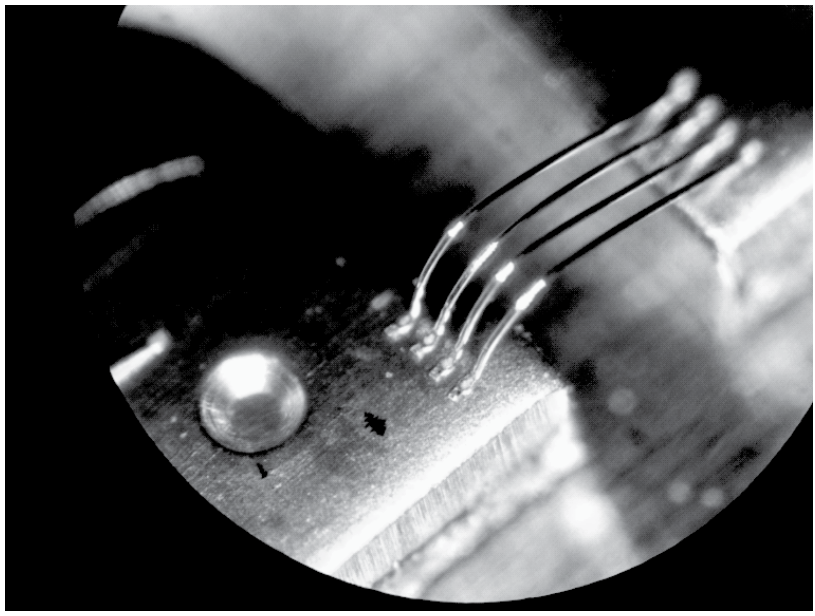


Figure 5.2 Four aluminum wire bonds have been placed with a wedge bonding tool. (Courtesy of WestBond, Inc., Anaheim, CA.)

between the wire and the metal surface. Thermocompression uses pressure from the bonding tool and high temperature to create the bond. Thermosonic bonding combines ultrasonic and thermocompression methods to create the bond. The most common wire bonds are the wedge and ball-and-stitch type. As can be seen in Figure 5.3(a), ball bonds get their name from the ball formed by the first bond. In this type of wire bond, the second bond is the stitch, which

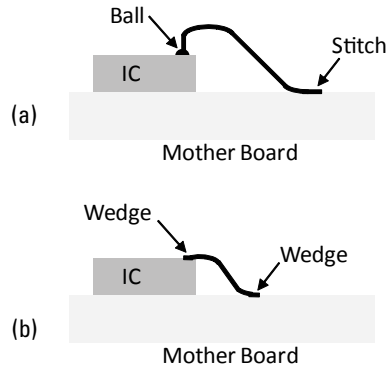


Figure 5.3 The most commonly used wire bonds are (a) ball bonds, which are also called ball and stitch bonds, and (b) wedge bonding.

connects to the motherboard or next level assembly. An important feature of the ball bond is the length of the wire that is required since the wire moves vertically from the ball before moving horizontally toward the stitch bond. The wedge bond [see Figure 5.3(b)] is a shorter length wire since it is able to move horizontally from the IC connection directly toward the second bond on the motherboard. As a result, wedge bonds are able to make connections from the motherboard to a pad that is physically closer to the IC, which further reduces the length of the wire bond. It is common for DC and low-frequency circuits to use ball-and-stitch bonds and higher frequency circuits often use wedge bonding.

5.1.2 Wire Bond Reliability

The reliability of a wire bond has many different aspects. One important aspect is the metallurgy of the wire itself. For instance, gold wire used for wire bonding is manufactured with small amounts of alloy material such as beryllium and is tempered under several different conditions. As a result, wire can be purchased based on its metal type (gold, aluminum, copper, and so on), its diameter (or width and thickness for ribbon bonding), elongation (%), tensile strength (g), break load (g), temper condition (hard, annealed, stress relieved, and so on), and other parameters.

Another important aspect to wire bond reliability is the setting of the wire bond machine used to place the wires. The bonding machine can be adjusted to control the temperature of the work surface, which sets the temperature of the part being wire bonded, the force used at the bonding head, the ultrasonic power, and the duration of the dwell for each bond. Two other important aspects of wire bond reliability, which will be addressed in more detail, are bond pull testing and wire bond-to-bond pad metallurgy.

One method for controlling the reliability of wire bonds is to measure the force required to break the bond between the wire and bonding pads. If this test is conducted in coordination with optimization of the wire bond process, it is possible to obtain wire bonds with high bonding strength. This is important because high-bond-strength wire bonds are less likely to fail. In fact, it is common for wire bond pull tests to be conducted periodically (e.g., at the start of a work shift and end of a work shift) by quality control personnel.

A wire bond pull tester machine is shown in Figure 5.4. Bond pull testing is the most universally accepted method for controlling the quality of wire bond operations. In fact, MIL-STD-883 Method 2011.7 is used extensively in the microelectronics industry as a procedure for testing the bond strength of wire bonds; it states that "The purpose of this test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specific bond strength requirements…" [1]. The wire bond pull tester uses a miniature

Figure 5.4 Wire bond strength is measured using a wire bond pull tester. (Courtesy of West-Bond, Inc., Anaheim, CA.)

hook to grab the wire bond and pull until the wire fails. The wire will stretch and either fail by pulling away from one of the bond pads or it will fail by the wire breaking. Figure 5.5 illustrates a wire bond before and during wire bond pull testing. Typical wire bond specifications show wire bond strength of at least 3g for a 0.0254-mm wire gold wire. However, a production environment typically can achieve 8g to 12g.

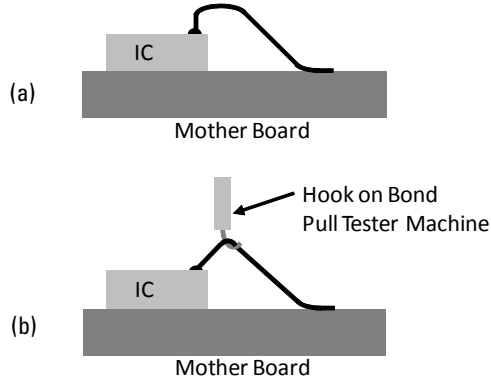


Figure 5.5 Illustration showing a wire bond (a) before bond pull testing and (b) during bond pull testing.

Another possibility for reliability concerns is the metallurgy of the wire bond-to-bond pad contact. For instance, gold wire bonds to aluminum bond pads [2] can be a concern due to the possible creation of gold-aluminum intermetallic compounds including purple plague ($AuAl_2$) and white plague (Au_5Al_2). These compounds, and other intermetallics, form at the interface of a gold wire bond and an aluminum bonding pad on an integrated circuit. Fortunately, these compounds form at high temperatures that are rarely encountered in high-frequency electronics. For storage at high temperatures, however, this effect can be a concern. Once these intermetallics form, they cause reliability and performance issues due to brittleness and reduced conductivity at the contact point.

In recent years, the use of copper wire has increased in microelectronic wire bonding processes due primarily to the rising cost of gold. The use of copper wire is now part of mainstream manufacturing processes, but there were hurdles to overcome for the adoption of copper wire [3]. One of the major obstacles to overcome in copper wire bonding is cratering and fracturing of the underlying pad structure. This is due to the hardness of copper metal compared to gold. The Vickers hardness of copper is about 1.72 times the Vickers hardness for gold (approximately 369 MPa for copper and 216 MPa for gold). Vickers hardness is a measure of a material's mechanical resistance to plastic deformation. Because copper is harder than gold, the ultrasonic power and force generated by the bonding machine must be higher, which causes failure at the bond pad. Other problems are pad metal peeling and aluminum pad metal push-out. Some solutions to this problem include the addition of tungsten (W) to the bond pad metallurgy for Al/Cu bond pads [4] and the use of NiPd and NiPdAu bond pads instead of standard Al pad finishes [5]. These alternative wire bond metallurgies improve the reliability of copper wire bonding.

5.1.3 Wire Bond Electrical Performance and Modeling

Electrical modeling of wire bonds requires specific information about the wire bond and the surrounding structures [6, 7]. Typically, the input parameters are the operating frequency (f), round wire radius (r_0), shape of the wire, metal conductivity (σ), and the dielectrics (ε_r) in the structure between the wire and ground. It is common to make the simplifying assumption that the actual wire shape is replaced by a series of straight wire sections to approximate the actual wire contour. This is the approach suggested in JEDEC Standard No. 59 and is used in much of the published work on wire bond modeling. Modern 3D electromagnetic simulation software allows for complex wire geometries to be generated and analyzed. Despite the flexibility offered by these software tools, most designers still approximate the actual wire bond contour within the simulator by sections of straight wires. This section focuses on the progressive devel-

opment of an equivalent electrical circuit of wire bond interconnects. This type of interconnect allows for greater modeling flexibility and improved insight into the electrical effects of wire bonds. We will show that as the model fidelity increases by accounting for additional parasitic effects, the agreement between HFSS simulations and the equivalent circuit increases.

To accurately model the wire bond interconnect, parasitic effects must be taken into account. Parasitic effects result from the fact that the wire bond discontinuity creates a significant disturbance to the propagating signal. This results in stray capacitance and inductance that must be included in any equivalent circuit that is developed. Fortunately, for many applications, these stray elements can be easily identified and circuit elements can be used to represent and model their effects.

The fundamental effect of a wire bond interconnect is an inductive discontinuity that causes an impedance mismatch between the circuits connected by the wire. As discussed later, it is possible to create a matching network to compensate for the impedance mismatches. However, before such a matching network can be created, an equivalent circuit and method for accurately modeling the wire bond is required.

5.1.4 Straight Wire Bond Between Substrates

The first wire bond we consider is the rather ideal case of a straight wire bond between two substrates, as shown in Figure 5.6. The figure is an image from a HFSS model. Note how the wire bond extends from the edge of one substrate to the edge of the other substrate. The wire diameter is *d*, the substrate thickness is *h*, and the length of the wire bond is equal to the spacing between substrates, which is *S*. To increase the fidelity of the model, a wedge-type bond with a flat bond contact is used. Figure 5.7 is a close-up view showing the wedge bond details. It is important to note that we assume the bond pad on the substrate, which is shown as transmission line length LMS, is included in the wire bond

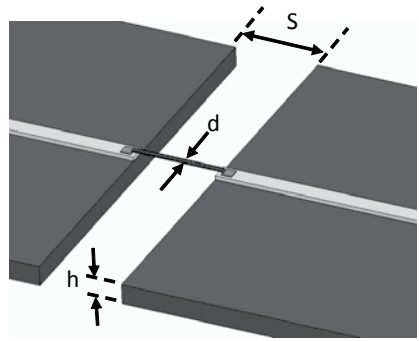


Figure 5.6 Straight wire bond between two substrates.

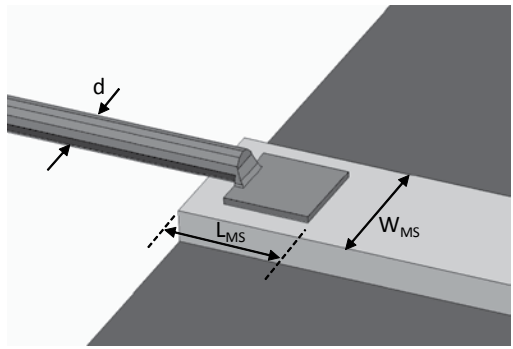


Figure 5.7 Details of wedge bond contact showing the section of microstrip line, LMS, that must be included for a high-fidelity model.

equivalent circuit. This extra extension of microstrip line must be taken into account for a high-fidelity model. As will be seen, we can divide the wire bond into several sections and analyze each section to obtain a high-fidelity model [8, 9].

The straight wire bond can be analyzed as an ideal wire over a ground plane. Figure 5.8 shows the side view and cross-sectional view of the straight wire bond. For additional usefulness, the figure shows a dielectric under the wire. However, for the straight wire case being considered, there is only air between the wire and the ground plane. For this case, we can calculate the line impedance of the wire over the ground plane using the following equation:

$$L_g \cong 2\ln\left(\frac{2H}{r}\right) nH/cm \tag{5.1}$$

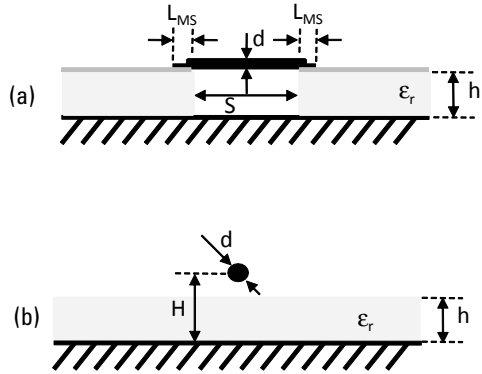


Figure 5.8 Simplified wire bond connection showing the (a) side view of a straight wire bond connection between two substrates with wire length L, wire diameter d, and substrate thickness h, and (b) cross-sectional view showing the wire bond over a dielectric substrate.

where we assume r << H and also:

L_g = inductance of a wire over a ground plane
H = distance of wire above the ground plane
r = radius of the wire.

As an example, a simulation of the straight wire bond interconnect was conducted in HFSS. In the model, the wire is 0.163 mm above the ground plane with a diameter of 0.0254 mm, and it is 0.75 mm long. A simple equivalent circuit of the straight wire bond was developed consisting of just a series inductor. By using (5.1), the wire bond inductance was calculated to be 0.489 nH. The HFSS simulation results and a circuit simulation using the simple series inductor equivalent circuit are compared in Figure 5.9. As can be seen, the

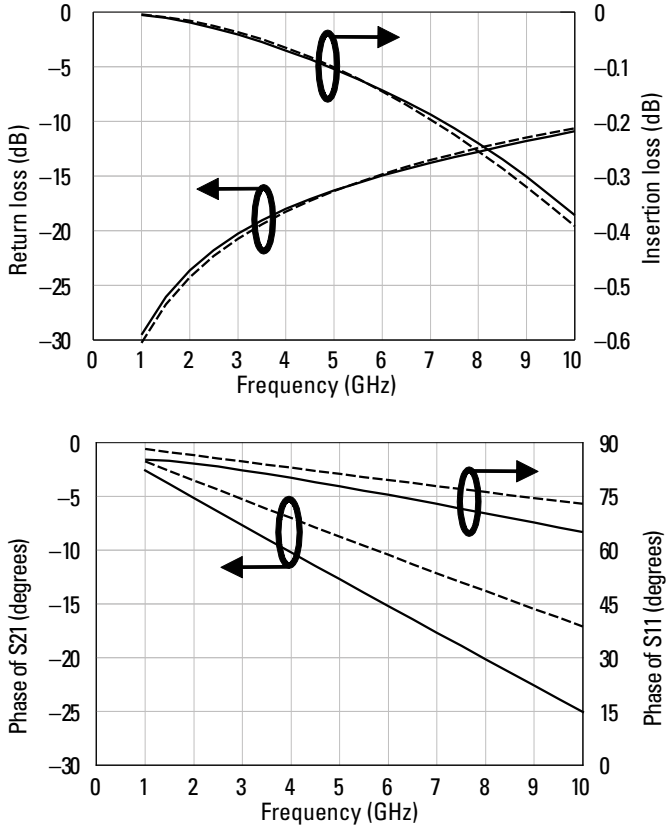


Figure 5.9 Comparison of a simple inductor equivalent circuit of the wire bond showing (a) magnitude of return loss and insertion loss in decibels, and (b) phase of S21 and S11 in degrees. (Note: The HFSS simulation uses solid lines; circuit simulation uses dashed lines.)

agreement using this simple model is good for the magnitude of the scattering parameters, but the agreement for the phase is off by as much as 8 degrees at 10 GHz. Although it is encouraging that such a simple model is able to capture much of the electrical effects in the band of interest, clearly, the fidelity using a simple series inductor as the equivalent model is not sufficient to capture all of the effects that contribute to the performance of the wire bond. Therefore, a more sophisticated equivalent circuit is required.

Consider the wire bond interconnect equivalent circuits shown in Figure 5.10. The figure shows increasingly complex wire bond models starting with the simple series inductor. A more complex model of the wire bond is also shown in the figure. It uses shunt capacitors C1 and C2 and a series resistor. A higher fidelity model includes the bonding pad effects as short sections of transmission lines of length, L_{MS} and impedance, Z_{MS}. The capacitors account for the parasitic capacitance that the wire bond generates. Actually, for this analysis, it is best to consider C1 and C2 to be the distributed effects of the wire bond when it is considered to be a transmission line. In this case of a physically symmetrical structure, the capacitors are equal. In some implementations of the equivalent circuit, the effects of the bond pads are absorbed into C1 and C2, which increases their value. If that approach is taken, the transmission lines in Figure 5.10(c) at the input and output (with length L_{MS}) are eliminated and the calculation of C1 and C2 will include the capacitance of the bonding pad. The resistor R_w is due to the finite conductance of the wire bond metal. One approach to calculating the element values for the model is to treat the wire bond as a transmission line. If the line impedance of the wire bond can be calculated, then the inductance and capacitance of the wire bond can be calculated and

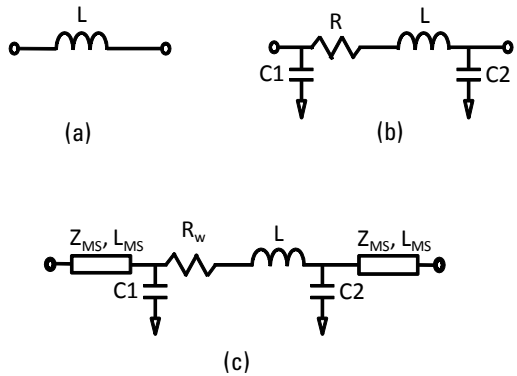


Figure 5.10 Increasingly complex wire bond equivalent circuits starting with the (a) simple series inductor appropriate for low-frequency simulations only, (b) a more complex model that takes into account more of the parasitic effects from the wire bonds, and (c) a high-fidelity model that accounts for many of the wire bond parasitic effects.

used in the model. The line impedance of a wire over a grounded dielectric slab [as shown in Figure 5.8(b)] is given as [10, 11]:

$$Z_{ow} = \frac{60}{\sqrt{\varepsilon_{reff}}} \cosh^{-1}\left(\frac{1-u^2}{2R} + \frac{R}{2}\right) \quad \text{ohms} \tag{5.2}$$

$$R = \frac{2}{\left(4H/a - a/H\right)} \tag{5.3}$$

$$u = \frac{1}{\left(2H/a\right)^2 - 1} \tag{5.4}$$

$$\varepsilon_{reff} = \frac{\ln\left(\frac{2H}{a}\right)}{\ln\left[\frac{2(H-h)}{a} + \frac{2h}{a\varepsilon_r}\right]} \tag{5.5}$$

where (see Figure 5.8):

Z_{ow} = impedance of the wire bond over a grounded dielectric slab
$a = d/2$ = radius of the wire bond
H = height of the wire bond
h = height of the substrate
$\varepsilon_{\text{reff}}$ = effective dielectric constant of the wire transmission line
ε_r = dielectric constant of the substrate between the wire bond and ground

The wire bond line impedance for the example above can be calculated using (5.2) by assuming that the dielectric constant ε_r is equal to 1 since there is only air (no dielectric) below the wire bond in this instance. For the example considered earlier (H = 0.163 mm, d = 0.0254 mm, and ε_r = 1), the line impedance of the straight wire bond is 195.58Ω.

An alternative to using (5.2) to calculate the line impedance for the case of a straight wire bond over a ground plane [as shown in Figure 5.8(b) but without the substrate] is to use:

$$Z_{ow} = 168 \cdot \log_{10}\left(\frac{4\mathrm{H}}{\mathrm{d}}\right) \quad \text{ohms} \tag{5.6}$$

The line impedance of the straight wire bond interconnect using (5.6) for H = 0.163 mm and d = 0.0254 mm is 194.32Ω, which agrees to within 1% with (5.2). Once the line impedance is known, we can then calculate the line inductance and the line capacitance (the derivation is left as an exercise):

$$L_{dist} = \frac{Z_{ow}\sqrt{\varepsilon_{reff}}}{v_o} \quad \mathrm{H/m} \tag{5.7}$$

$$C_{dist} = \frac{\sqrt{\varepsilon_{reff}}}{Z_{ow} v_o} \quad \mathrm{F/m} \tag{5.8}$$

where:

v_0 = free-space velocity = 3 × 108 m/s
L_{dist} = distributed line inductance (H/m)
C_{dist} = distributed line capacitance (F/m).

Using (5.7) and (5.8), we can determine the inductance and capacitance to use in the equivalent circuits. The line inductance is 651.9 nH/m and the line capacitance is 17.04 pF/m. The inductance of the wire bond line is found by multiplying the distributed inductance by the length of the wire: $L = S \times L_{dist}$. The same holds true for the capacitance of the wire bond interconnect: $C = S \times C_{dist}$. For a wire bond length of $S = 0.75$ mm, this results in $L = 0.489$ nH and $C = 0.0127$ pF (C1 = C2 = $C/2 = 0.0064$ pF). As a confirmation of this method, note that the inductance L agrees with the inductance calculated using (5.1).

The resistive part of the wire bond model is due to the finite conductivity of the metal that is the wire bond. The DC resistance of the wire bond is given by

$$R_W = R_{DC} = \frac{S}{\sigma A} \quad [\Omega] \tag{5.9}$$

where:

S = spacing between substrates = wire bond length (m)

σ = conductivity of the wire (s/m)

A = cross-sectional area of the wire bond = $\pi a^2/(m^2)$

a = radius of the wire bond = d/2 (m).

For a gold wire with a conductivity of 4.1×10^7 mho/m, the DC resistance of the wire is 0.036Ω. The resistance adds a small effect at low frequencies.

When the effects of the microstrip bonding pad are included, the modeling fidelity is increased significantly. Figure 5.11 shows the agreement between the HFSS simulations of the wire bond and the high-fidelity equivalent circuit from Figure 5.10(c). The element values for the model are repeated below for clarity:

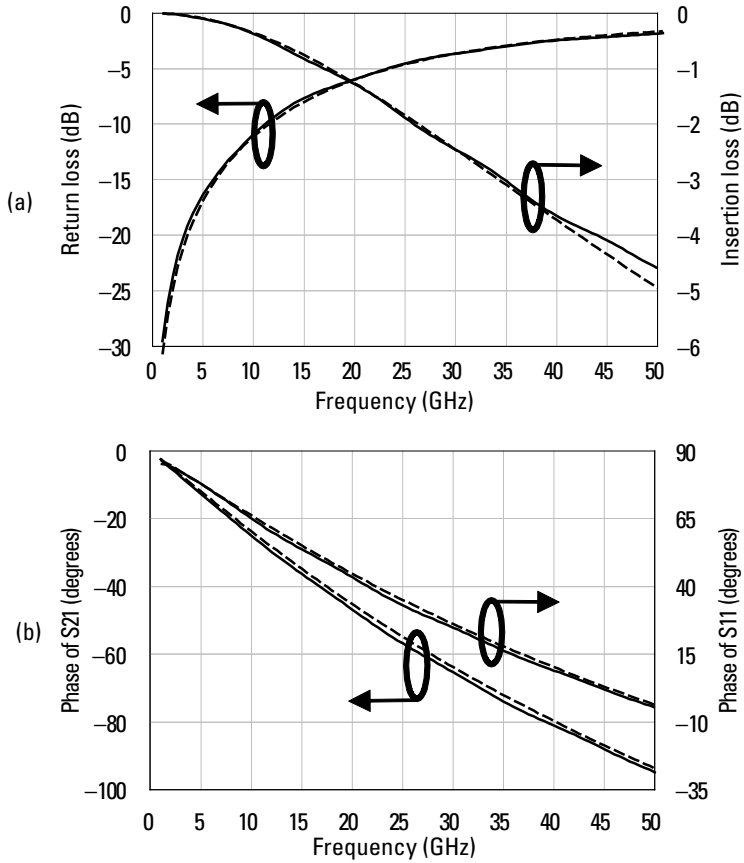


Figure 5.11 Comparison between HFSS simulation and the high-fidelity equivalent circuit model for a straight wire bond interconnect. (Note: The HFSS simulation uses solid lines; equivalent circuit uses dashed lines.)

$L = 0.489$ nH

C1 = C2 = 0.0064 pF

$R = 0.036\Omega$

$L_{MS} = 0.090$ mm

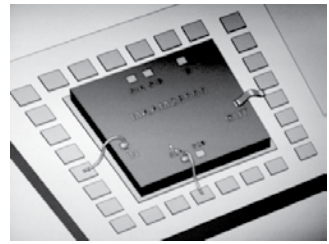
$Z_{MS} = 50.2\Omega$ ($\varepsilon_{\text{reff}} = 6.01$)

Although a simple and accurate equivalent circuit of the wire bond can be developed, a straight and flat wire bond is not practical. This is due the fact that wire bonds require a loop for stress relief between components. Therefore, the next section addresses the analysis of modeling wire bonds that are typically encountered in real-world applications.

5.1.5 Wire Bond Between an MMIC and Substrate

The next wire bond that we consider is between an MMIC chip and a motherboard using a ball-and-stitch bond. Figure 5.12(a) illustrates an MMIC mounted onto a low-cost laminate package with wire bonds for an actual product. High-fidelity modeling of this bond requires more sophistication than what was used in the previous section for modeling of the straight wire bond. This is due to the fact that the wire bond has a contour to its shape that must be correctly accounted for. In this section, we expand on the method developed in the previous section to analyze this wire bond. An HFSS simulation was conducted on the wire bond shown in Figure 5.12. The wire bond approximates the actual

(a)



(b)

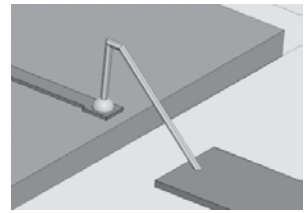


Figure 5.12 Ball-and-stitch wire bonding is very typical in volume production for (a) MMIC interconnects to packages and (b) the wire bond can be approximated by straight line segments for HFSS analysis.

wire bond contour using straight line segments. An equivalent circuit for this circuit can be developed to model the wire bond.

The cross-sectional view of the wire bond is shown in Figure 5.13(a). Note how the wire bond is approximated by a series of line segments that can be independently analyzed. The contribution from each section can then be added to obtain the complete electrical model.

A high-fidelity equivalent circuit is shown in Figure 5.13(b). It shows that the wire bond pad models include a section of line of impedance Z_{BP} for the bond pad on the MMIC and Z_{MB} for the bond pad on the motherboard. In addition, the bond pad model uses an open end section to account for the extra capacitance off the end of each bond pad. Standard circuit simulator models for these elements are well established and capable of modeling the bond pads with $\varepsilon_r = 12.9$ at a thickness of 0.101 mm and a line pad size of 0.101 mm × 0.101 mm for the MMIC substrate, and $\varepsilon_r = 6.15$ and thickness of 0.254 mm and pad size of 0.356 mm × 0.065 mm for the motherboard. The wire section LW1 is modeled with a series inductor L_{LW1} and a parasitic capacitance C_{par}. It is due to stray capacitance from the wire to the MMIC dielectric. It is determined through circuit model matching to measured data or electromagnetic simulations.

The other two wire sections are modeled by transmission lines of impedance Z_{LW2} and Z_{LW3}. Finally, a lumped resistor models the effect of the finite conductor loss of the wire bond. Since the wire section LW2 is modeled as a

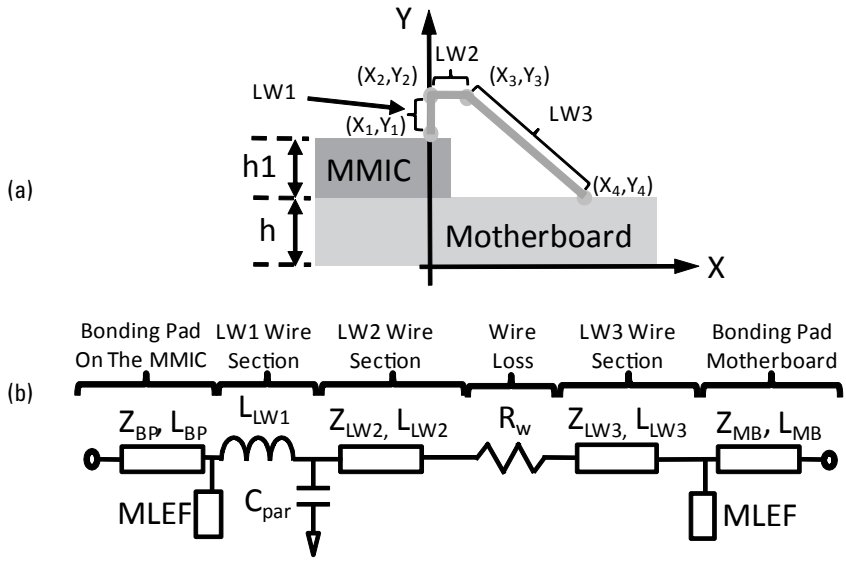


Figure 5.13 Cross-sectional view of the wire bond shows that it is (a) made up of line segments LW1, LW2, and LW3 with an (b) equivalent circuit of inductors and capacitors.

transmission line, (5.2) and (5.5) can be used to calculate the line impedance and effective dielectric constant. The wire section LW3 is not horizontal but instead slopes down to contact the motherboard. For ease of simulation, wire section LW3 is modeled assuming that a horizontal line section is placed between the vertical positions at Y_3 and Y_2. This allows the use of (5.2) and (5.5) to calculate the impedance and effective dielectric constant of LW3.

The first step in calculating the equivalent circuit is to determine the inductance of LW1. This section extends vertically and we will make the simplifying assumption that it can be modeled as a purely inductive wire. In this case the inductance is given as:

$$L_w = 2\text{Length}\left[\ln\left(\frac{2\text{Length}}{r}\right) - 1\right] nH \tag{5.10}$$

where:

L_w = inductance of a wire in free space
length = wire length (cm)
R = wire radius

The inductance of LW1 was found to be 0.135 nH using (5.10). Next, the transmission line parameters of LW2 and LW3 were calculated using (5.2) and (5.5). The model values are:

$L_{LW1} = 0.135$ nH
$Z_{LW2} = 267.9$ mm
$E_{reff(LW2)} = 1.092$
$\text{length}_{LW2} = 0.051$ mm
$Z_{LW3} = 235.2$ mm
$E_{reff(LW3)} = 1.168$
$\text{length}_{LW3} = 0.503$ mm

The results are shown in Figure 5.14. Note that the agreement between the HFSS simulation and the equivalent circuit is very good for both the magnitude and phase of the scattering parameters.

5.1.6 Ground Current Parasitics in Wire Bonded Circuits

For most millimeter-wave applications, ground currents in wire bonded interconnects must be taken into account to avoid unexpected issues. Parasitic

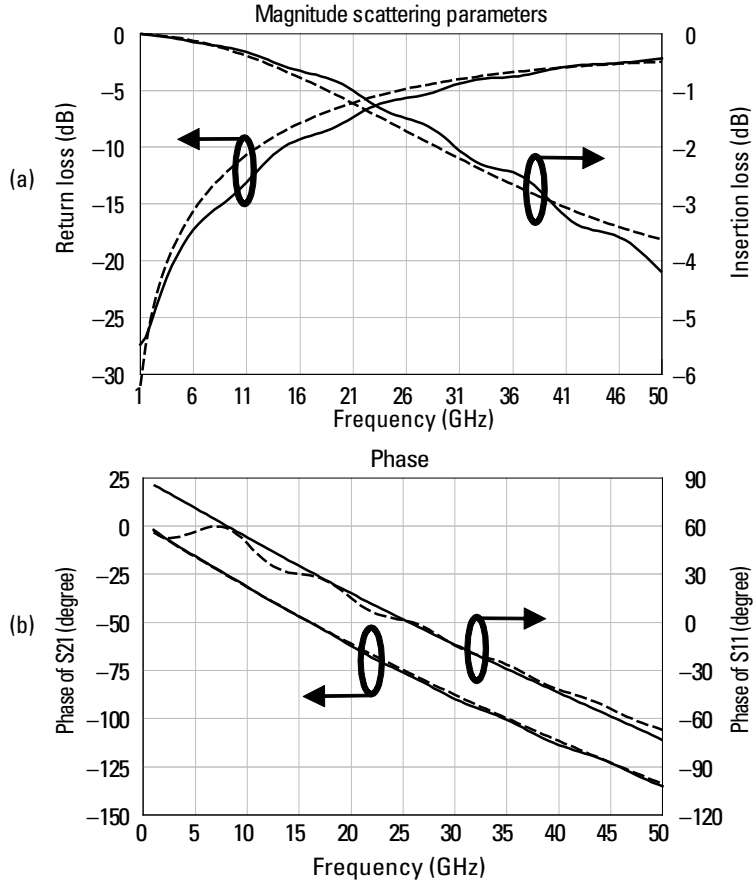


Figure 5.14 Comparison of the HFSS and equivalent circuit simulations for a ball bond interconnect showing (a) the magnitude of return loss and insertion loss in decibels and (b) the phase of S21 and S11 in degrees. (Note: The HFSS simulation uses solid lines; circuit simulation uses dashed lines.)

effects in the signal line for wire bond contacts are important, but unexpected ground paths can cause significant parasitic effects similar to adding a series inductor in the signal path. Consider the configuration shown in Figure 5.15. It shows an MMIC with a wire bond connection to an LTCC substrate. The MMIC is attached to a high thermal conductivity CuW shim to improve heat dissipation. The LTCC substrate is attached to a Kovar metal base for added mechanical strength. Both are attached to the package ground plane. In this configuration, note that the signal path is along the transmission line on the MMIC to the bond pad and through the wire bond to the LTCC substrate and out to other circuits. However, the ground signal must travel down from the CuW shim to the housing metal ground over to the Kovar base and up to

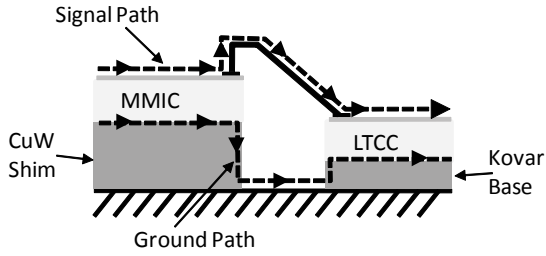


Figure 5.15 Illustration of the ground signal path of a wire bond.

the LTCC ground plane. This signal path that the ground current must travel introduces an inductive effect. This can be a particularly significant problem for some type of IC packages on PCBs [12] and millimeter-wave hybrids with pedestal-mounted MMICs.

5.1.7 Tuning Wire Bond Interconnects

Wire bond interconnects tend to have limited bandwidth due to their series inductance. However, this series inductance can be tuned out using a matching circuit on chip and/or on the motherboard. Figure 5.16(a) illustrates a tuning circuit used to match the impedance of the wire bond over a wide bandwidth. In this instance, a two-section matching network is being used. The first section, nearest the wire bond, is capacitive and the second section is inductive. Figure 5.16(b) shows the before and after return loss. The 15-dB return loss bandwidth is approximately 10 GHz before tuning and approximately 20 GHz after tuning. This matching technique has been successfully been applied to over 120 GHz [13].

5.1.8 Other RF Uses for Wire Bonds

In addition to making signal interconnects, wire bonds can be used for many different applications. For instance, wire bonds have been used as tuning elements in microwave hybrid circuits for many decades. One interesting use of wire bonds for tuning is for filters [14]. In this instance, wire bonds are connected between capacitive circuit elements so that the shunt capacitance of the filter can be varied. The wires can be added to adjacent capacitive pads to connect them to the rest of the circuitry. This allows the shunt capacitance to increase or decrease.

Wire bonds have also been used to create circuit elements in filters and couplers. The inductive nature of the wire bond makes it convenient to realize a series or shunt inductance. Another application is in the realization of a miniature branch-line coupler slow-wave structure [15]. In this circuit, the wire

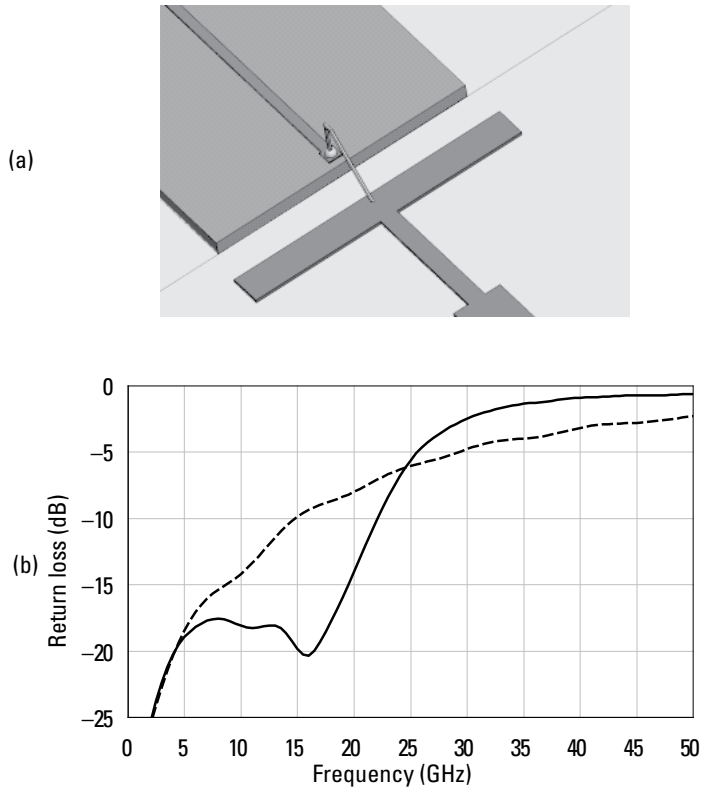


Figure 5.16 Electrical compensation of the wire bond is possible with (a) matching circuits, and (b) the benefit is improved bandwidth. (Note: Dashed line is before compensation; solid line is after compensation.)

bonds are used as series inductive elements connected between shunt capacitive pads. This slow-wave structure is used to reduce the overall size of the coupler, and wire bonds provide the require series inductance.

Wire bonds have even been proposed for use as transmission lines in a coplanar structure [16]. In this approach, three wire bonds are placed parallel to each other. The capacitance between the wires serves to lower the impedance and create a coplanar waveguide structure. Because of the limited amount of capacitance that can be realized between the wires, the line impedance tends to be high. However, for some applications this may provide a useful advantage. For instance, this may be useful to avoid ground loop problems in some circuits. By moving the ground to the top of an IC and the motherboard as a type of coplanar waveguide contact, ground loop issues can be minimized.

As mentioned previously, at the right frequency, a wire bond will perform like an antenna. Normally, this is an undesirable effect of a wire bond. However, some have made use of this and intentionally designed antennas out of

wire bonds [17]. At 60 GHz the wavelength is short enough that a small wire bond can be a resonant antenna. Figure 5.17 illustrates the wire bond antenna structure. Note how the antenna is fed from a differential signal pair, which is wire bonded to a trace on the substrate. It forms a loop antenna with a reported VSWR of less than 2:1 over a 14% bandwidth with 0-dBi gain. The benefit of this approach is that it achieves a very low cost antenna at 60 GHz. The drawback is that antenna performance is dependent on the accuracy of the wire bond placement and shape of the loop. If these variables can be controlled in production, then this may be a viable, unique use for wire bonds.

While wire bonds are traditionally used to connect signals and bias between ICs or between substrates, it is clear that wire bonds can be used in many different applications.

5.2 Ribbon Bonding

Ribbon bonding is the same as wire bonding except that ribbon bonds have a rectangular cross section rather than circular. Figure 5.18 shows a comparison of a millimeter-wave IC mounted onto a substrate and interconnected using wire bond and ribbon bonds for the RF signal paths. In both cases, the low-frequency interconnects use wire bonds; it is only the RF interconnects that use ribbon bonds. Ribbon bonds are widely used in high-speed telecom modules and millimeter-wave applications. This is due to their lower inductance compared to a wire bond. Figure 5.19 shows the input return loss for a straight wire bond and a ribbon bond over a ground plane 0.254 mm below the wires.

5.3 Flip Chip Interconnects

Flip chip interconnects have been extensively used for many decades for low-frequency applications in high-end microprocessors and in the automotive industry. However, the use of flip chips at microwave and millimeter-wave

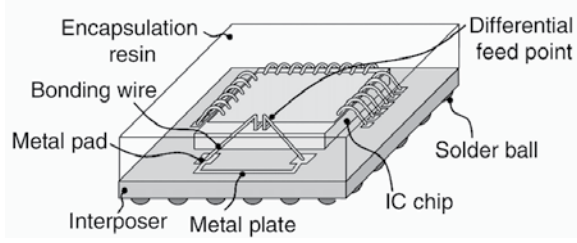


Figure 5.17 Wire bonds can be used as part of an antenna. (© 2013 IEEE. From: [17]. Reprinted with permission.)

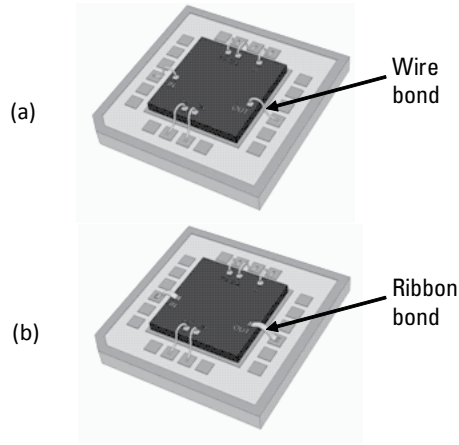


Figure 5.18 Model of ribbon and wire bonding onto a chip package.

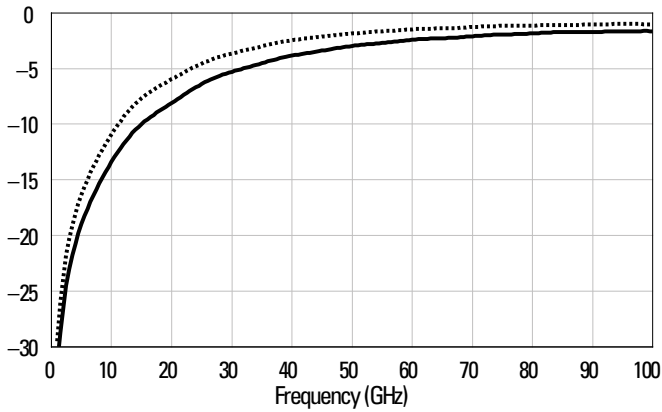


Figure 5.19 HFSS simulation results showing the difference between a 0.0254-mm-diameter wire bond (dashed lines) and a 0.076-mm × 0.0125-mm ribbon bond (solid line for return loss) for a 0.75-mm-long straight connection between 0.254-mm-thick substrates.

frequencies requires paying attention to details that are not encountered in low-frequency applications. As will be seen, the additional concerns include proper design of the transmission lines involved, avoidance of parasitic modes, and the careful placement of isolation and grounding vias to reduce the appearance of undesired resonances and coupling. Despite the challenges, flip chip interconnects are particularly useful at microwave and millimeter-wave frequencies because of the lower inductance and tight manufacturing tolerances that can be achieved. Other benefits for GaAs MMIC flip chips are that full-thickness die can be used, which eliminates processing steps and provides for a more robust chip for high-speed assembly. Figure 5.20 is a side view illustration of a flip

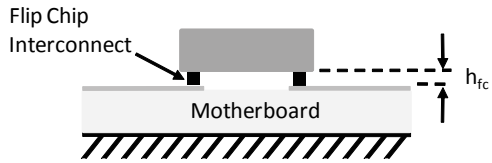


Figure 5.20 Illustration of the flip chip interconnect showing the spacing between the flip chip and the motherboard as hfc.

chip integrated circuit mounted to a motherboard. Note that the flip chip interconnect provides the dual purpose of electrical interconnect and mechanical attachment of the integrated circuit. Some of the earliest uses of flip chips for high-volume MMICs were for transmit/receive modules in phased-array radar modules [18–20].

Flip chip interconnects for ICs were first developed by IBM for use in their mainframe computers in the 1960s. Delco Electronics used flip chips for automotive electronic modules in the 1970s and 1980s. Since Hughes Aircraft Company was a sister company to Delco electronics, in the late 1980s, flip chip technology was adopted by Hughes for use as an MMIC interconnect for phased-array radar modules. Currently, flip chips are widely used in rf applications such as mobile phones, millimeter-wave communication systems, and radar systems.

5.3.1 Types of Flip Chip Interconnects

There are many different types of flip chip interconnects. Figure 5.21 illustrates a few of the flip chip interconnects currently in use. A solder bump flip chip interconnect is shown in Figure 5.21(a). It is difficult to count the number of variations on solder bump interconnects. The pioneer in this technique was IBM. Their technique is named Controlled Collapse Chip Connection (C4). The majority of flip chips are fabricated using some variation of solder bumps.

The hard bump flip chip interconnect is illustrated in Figure 5.21(b). In this configuration, a metal bump, normally of silver or gold, is grown on the IC interconnect pads. The connection to the motherboard is achieved using solder. The metallurgy of the hard bump solder attachment is an important design consideration.

Stud bumps are illustrated in Figure 5.21(c) just prior to thermosonic attachment. The stud bump can be understood as half of a ball-and-stitch wire bond except that only the first bond is connected. In this approach, the stud bump is created and then the wire is broken instead of making a second connection. Figure 5.22(a) is an image of a stud bump before connection. Note the tapper at the top of the stud bump caused by the intentional breaking of the wire. The stud bump is normally placed on the bond pads of the integrated

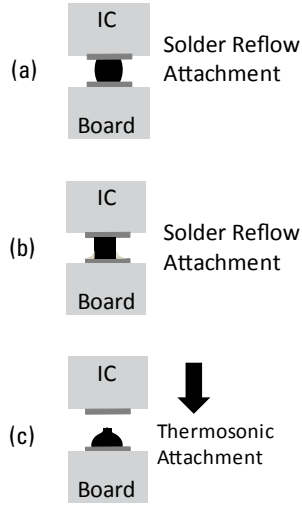


Figure 5.21 Three of the most common flip chip interconnects: (a) solder bump, (b) hard bump that is solder attached, and (c) stud bump.

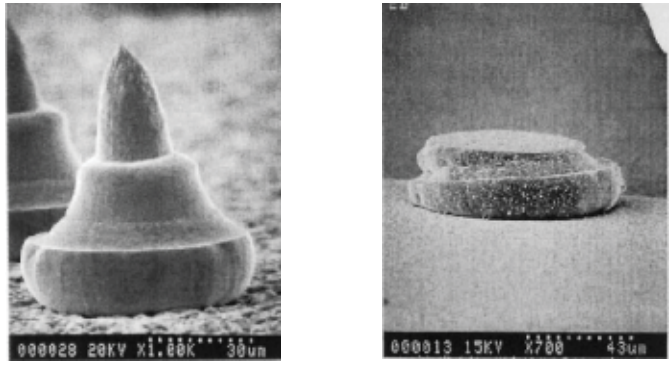


Figure 5.22 A stud bump (a) before and (b) after attachment. (From: [24]. © 2000 IEEE. Reprinted with permission.)

circuit. Figure 5.21(b) shows the collapsed stud bump after thermosonic attachment (with IC removed).

5.3.2 Electrical Modeling of Flip Chip Interconnects

Early in the development of flip chips using GaAs MMIC processing, it was unclear which transmission line was optimum for use on the IC. A coplanar waveguide was chosen for most applications due to the fact that it offers easy

access to ground on the same surface as the active devices, allows high-performance electrical transitions, and allows for full-thickness wafers to be used, which results in reliable assembly. Several investigators have worked to develop equivalent circuits of the flip chip interconnect [21–23] and to determine design rules for implementation [24].

The main parameters affecting flip chip interconnects are shown in Figure 5.23 and are the bump pad on the IC (L_{PIC}), the bump pad on the motherboard (L_{PMB}), the diameter of the bump (D_{BUMP}), and the thickness of the bump (h_{BUMP}). It is important to note that the thickness of the bump is assumed to be the same as the gap between the substrate and IC including metal thickness and any attachment material such as solder, *z*-axis film, or epoxy. In most applications, L_{PMB} and L_{PIC} will not be the same since the precision of the processing on the IC is much higher than for the motherboard where the L_{PIC} is smaller than L_{PMB}. Parameters such as the thickness of the IC die (h_{IC}) and thickness of the motherboard (h_{MB}) have minimal effect on the transition performance of the flip chip interconnect (see, for instance, [24]). The exception to this is that at millimeter-wave frequencies the thickness of the IC has a second-order effect on a parasitic mode that can exist within the dielectric material of the MMIC. In addition, the thickness of the motherboard has a minor effect on very thin motherboards since the ground plane below the motherboard (and any circuits or signal routing) can couple to the signal lines on the IC. The extension of the IC beyond the IC bump pad (L_{EXT}) has a minor effect of adding capacitance to the transmission line on the motherboard.

The effect of the bump pad on the motherboard and on the IC creates a shunt capacitive discontinuity. This is a major contributor to the overall bandwidth of the transition for carefully designed transmission lines so that other impedance mismatches can be neglected. Heinrich, Jentzsch, and Baumann [22] found that the transition can be accurately modeled using a simple shunt capacitance model. In their approach, they compared simulations using the

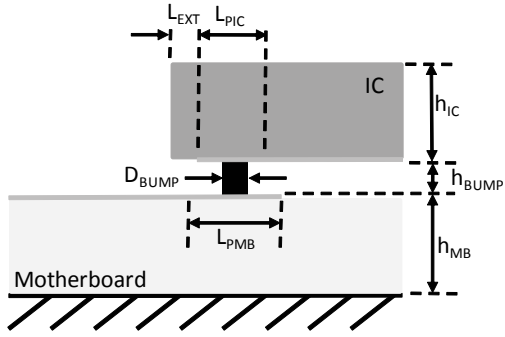


Figure 5.23 Illustration of the flip chip transition showing the important dimensions.

finite difference time domain method to a simple lumped capacitor model and demonstrate that a simple model using the closed-form capacitor equation provides sufficient accuracy.

The proximity of the substrate to the flip chip will affect the transmission lines on the IC [25, 26]. The distance between the mounting substrate and the IC is determined by the height of the bump, h_{fc}. If the height of the bump is allowed to vary and all other parameters remain the same, the line impedance of the IC coplanar waveguide line will be reduced as the bump height is reduced. Figure 5.24 shows the cross section of a CPW transmission line with multiple dielectric layers. This structure can be used to analyze the effect of the mounting substrate on CPW flip chips. Analytical expressions for transmission lines with multiple layers have been developed [27] that are useful in the analysis of coplanar waveguide line impedance and effective dielectric constant before and after IC mounting onto a motherboard:

$$C_{CPW} = C_0 + C_1 + C_2 + C_3 + C_4 + C_5 \tag{5.11}$$

This equation directs us to determine each of the line capacitance contributions and sum them to obtain the total capacitance of the CPW line. First, determine C0:

$$C_0 = 4\varepsilon_0 \frac{K'(k)}{K(k)} \tag{5.12}$$

where:

K= complete elliptical integral of the first kind

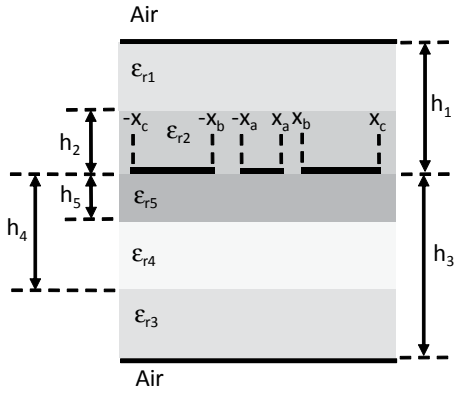


Figure 5.24 Multilayer CPW line. (© 1997 IEEE. After: [27]. Used with permission.)

$K'(k) = K(k')$

$$k = \frac{x_c}{x_b}\sqrt{\frac{x_b^2 - x_a^2}{x_c^2 - x_a^2}} \tag{5.13}$$

$$k' = \sqrt{1 - k^2} \tag{5.14}$$

For determining C1,

$$C_1 = 2\varepsilon_0(\varepsilon_1 - 1)\frac{K'(k_1)}{K(K_1)} \tag{5.15}$$

$$k_1 = \frac{\sinh\left(\frac{\pi x_c}{2h_1}\right)}{\sinh\left(\frac{2x_b}{2h_1}\right)}\sqrt{\frac{\sinh^2\left(\frac{\pi x_b}{2h_1}\right) - \sinh^2\left(\frac{\pi x_a}{2h_1}\right)}{\sinh^2\left(\frac{\pi x_c}{2h_1}\right) - \sinh^2\left(\frac{\mu x_a}{2h_1}\right)}} \tag{5.16}$$

$$k_1' = \sqrt{1 - k_1^2} \tag{5.17}$$

Now, we obtain the equations for C2 through C5:

$$C_2 = 2\varepsilon_0(\varepsilon_{r2} - \varepsilon_{r1})\frac{K'(k_2)}{K(k_2)} \tag{5.18}$$

$$C_3 = 2\varepsilon_0(\varepsilon_{r3} - 1)\frac{K'(k_3)}{K(k_3)} \tag{5.19}$$

$$C_4 = 2\varepsilon_0(\varepsilon_{r4} - \varepsilon_{r3})\frac{K'(k_4)}{K(k_4)} \tag{5.20}$$

$$C_5 = 2\varepsilon_0 \left(\varepsilon_{r5} - \varepsilon_{r4}\right) \frac{K'\left(k_5\right)}{K\left(k_5\right)} \tag{5.21}$$

where:

$$k_i = \frac{\sinh\left(\frac{\pi x_c}{2h_i}\right)}{\sinh\left(\frac{\pi x_b}{2h_i}\right)} \sqrt{\frac{\sinh^2\left(\frac{\pi x_b}{2h_i}\right) - \sinh^2\left(\frac{\pi x_a}{2h_i}\right)}{\sinh^2\left(\frac{\pi x_c}{2h_i}\right) - \sinh^2\left(\frac{\pi x_a}{2h_i}\right)}} \tag{5.22}$$

$$k_i' = \sqrt{1 - k_i^2} \tag{5.23}$$

Now, since the effective dielectric constant is equal to the ratio of the line capacitance with dielectrics present and line capacitance without dielectrics present, we can write [28]

$$\varepsilon_{reff} = \frac{C}{C_0} \tag{5.24}$$

$$v_{ph} = \frac{v_0}{\sqrt{\varepsilon_{reff}}} \tag{5.25}$$

$$Z_0 = \frac{1}{Cv_{ph}} \tag{5.26}$$

where:

C = line capacitance with dielectrics (F/m)
C_0 = line capacitance without dielectrics (F/m)
Z_0 = line impedance (ohms)
v_{ph} = phase velocity (m/s)
$\varepsilon_{\text{reff}}$ = effective dielectric constant
v_0 = speed of light in free space (m/s).

Substituting (5.11), (5.12), (5.15), and (5.18) through (5.21) into (5.24) results in

$$\varepsilon_{reff}^{CPW} = \frac{C_{CPW}}{C_o} = 1 + \frac{1}{2}(\varepsilon_{r1} - 1)\frac{K(k)K(k_1')}{K(k')K(k_1)} + \frac{1}{2}(\varepsilon_{r2} - \varepsilon_{r1})\frac{K(k)K(k_2')}{K(k')K(k_2)} + \frac{1}{2}(\varepsilon_{r3} - 1)\frac{K(k)K(k_3')}{K(k')K(k_3)} + \frac{1}{2}(\varepsilon_{r4} - \varepsilon_{r3})\frac{K(k)K(k_4')}{K(k')K(k_4)} + \frac{1}{2}(\varepsilon_{r5} - \varepsilon_{r4})\frac{K(k)K(k_5')}{K(k')K(k_5)} \tag{5.27}$$

Using (5.25) and (5.26), we obtain

$$v_{ph}^{CPW} = \frac{v_0}{\sqrt{\varepsilon_{reff}^{CPW}}} \quad [\text{m/s}] \tag{5.28}$$

$$Z_0^{CPW} = \frac{30\pi}{\sqrt{\varepsilon_{reff}^{CPW}}}\frac{K(k)}{K(k')} \quad [\Omega] \tag{5.29}$$

Using (5.27) and (5.29) and properly choosing which layers to assign, we can analyze the effective dielectric constant and line impedance of the CPW line as a function of spacing between the IC and motherboard.

An alternative is to use a commercial electromagnetic simulator such as HFSS. Figure 5.25 shows the CPW transmission line that was analyzed. Note that the lower CPW lines on the motherboard are shown only to clarify the definition of h_{BUMP}, but were not part of the analysis. The only conductors in the analysis are the CPW lines on the IC.

Figure 5.26 shows the results of an analysis conducted at 20 GHz. The values of the variable used in the analysis are as follows: line width of CPW line = 0.08 mm, gap of CPW line = 0.065 mm, thickness of IC conductors = 0.005 mm, thickness of motherboard lines = 0.0125 mm, thickness of the IC substrate = 0.5 mm with a dielectric constant of 12.9, and thickness of the motherboard is 0.254 mm with a dielectric constant of 6.16 (RO3006) for configurations 1 and 2 and 8.8 (aluminum nitride) for configuration 3. Note that the effect of the proximity of the motherboard is a reduction in line impedance

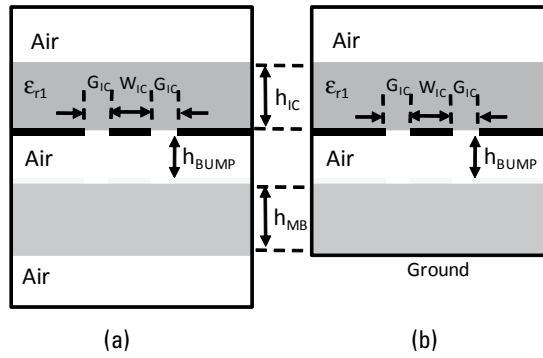


Figure 5.25 Two configurations of a CPW IC mounted to a motherboard were analyzed: (a) with air below the motherboards and (b) with ground below the motherboard.

and an increase in the effective dielectric constant. Above about 0.1 mm of bump height, the effect of the motherboard is negligible.

A set of HFSS simulations was conducted to determine the effect on return loss for various bump heights using the same configuration as for Figure 5.26. The results of the analysis are shown in Figure 5.27. Note that as bump height h_{BUMP} is decreased, the return loss is degraded.

5.3.3 Parasitic Modes in Flip Chip Interconnects

Several parasitic modes can be created in a MMIC flip chip interconnect. One mode is due to the existence of the undesired parallel plate mode in the CPW transmission line. In most practical realizations of packaging using flip chips, a ground is present under the coplanar waveguide lines. This ground plane is important because it provides isolation to other circuits, bias, and control line routing. However, as Liu, Cha, and Itoh determined [29], a conductor-backed coplanar waveguide has a zero cutoff mode that can lead to undesired resonance if not properly grounded. This mode can exist on the CPW line in the motherboard and also on the CPW line on the IC. The transition from the motherboard to the IC excites this undesired mode, which creates a forward (PPL2) and reverse (PPL1) propagating parallel plate mode [22] as can be seen in Figure 5.28. PPL1 is the parallel plate mode that propagates back toward the motherboard CPW line, and its effect can be minimized by using vias connecting the topside ground plane to the bottom side ground plane on the CPW in the motherboard. However, PPL2 which is the parallel plate mode that exists between the CPW line in the IC and the ground plane in the motherboard, is difficult to suppress. There is strong coupling between the desired CPW mode and the PPL2 mode; it can be as high as 30 dB. This can be a serious concern

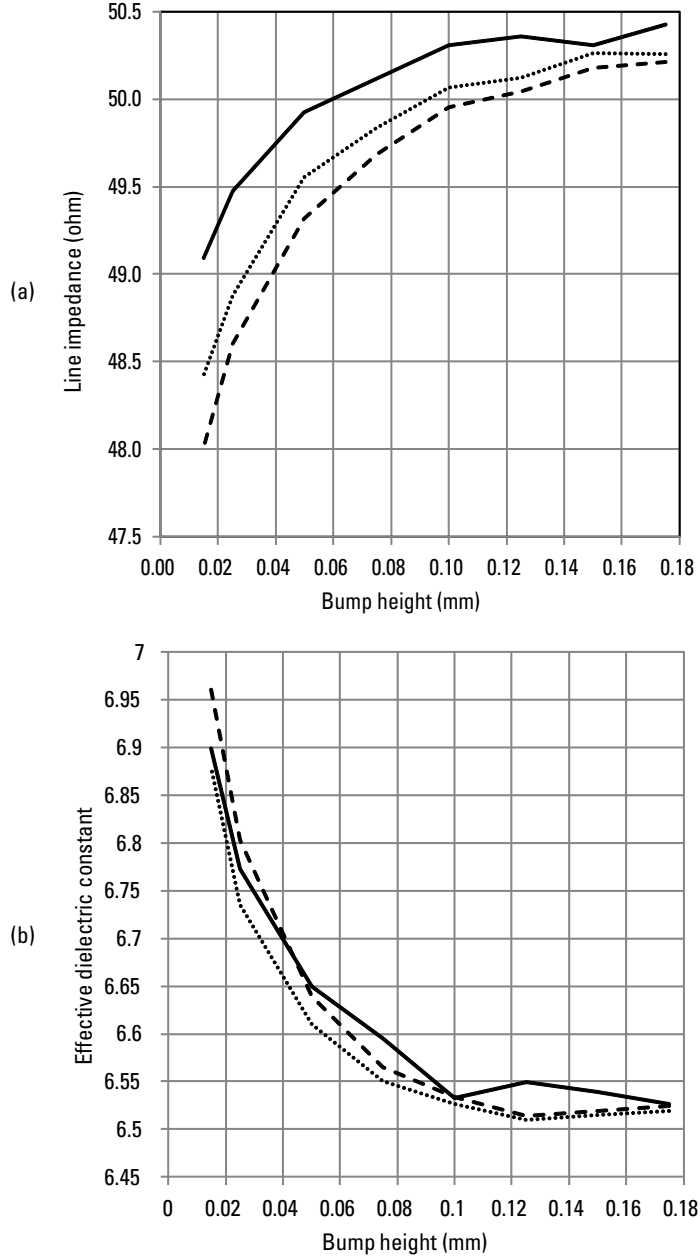


Figure 5.26 Proximity effect of a coplanar waveguide IC and the attachment substrate (a) for line impedance and (b) effective dielectric constant. [Note: Solid line = no ground below the motherboard as in Figure 5.25(a); dotted line = with a ground plane below the motherboard as shown in Figure 5.25(b) with a motherboard dielectric constant of 6.15; dashed line = with a ground plane below the motherboard as shown in Figure 5.25(b) with a motherboard dielectric constant of 8.8.)

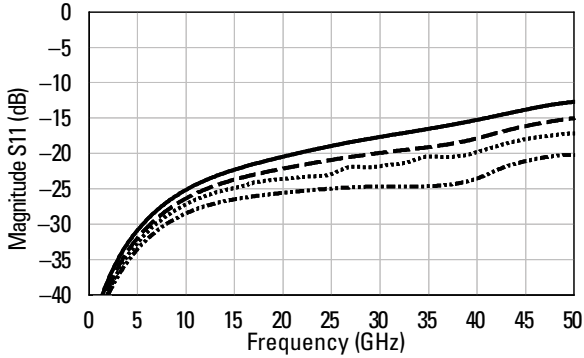


Figure 5.27 The configuration shown in Figure 5.23 was subjected to HFSS analysis for several different bump heights (h_{BUMP}) of 0.025, 0.05, 0.075, and 0.1 mm. (Note: Solid line = 0.025 mm; dashed line = 0.05 mm; dotted line = 0.075 mm; dotted and dashed line = 0.1 mm.)

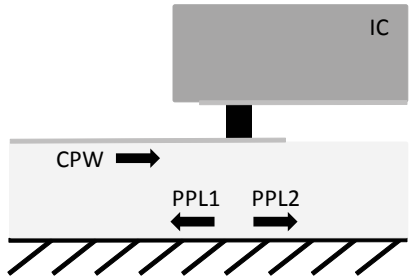


Figure 5.28 The transition between the CPW line on the motherboard and IC generates the parasitic parallel plate mode that propagates forward and reverse from the transition. (From: [22]. © 1998 IEEE. Reprinted with permission.)

for high-gain ICs and other adjacent circuitry, requiring careful design of the MMIC chip and the adjacent circuitry.

A parasitic resonance can occur at the transition from the motherboard to the MMIC if the CPW ground pad vias are not properly placed. In most practical realizations, the motherboard CPW lines will use a conductor-backed coplanar waveguide with grounding vias connecting the topside ground to the bottom side ground. The ground via closest to the bump interconnect must be placed close enough to avoid a possible quarter-wave resonance that can occur in the PPL1 mode. The line length LMV as shown in Figure 5.29 appears as a quarter-wave stub that is open on one end and short circuited on the other with a resonant frequency of

$$f_{MV} = \frac{v_o / \sqrt{\varepsilon_{rMB}}}{4 L_{MV}} \tag{5.30}$$

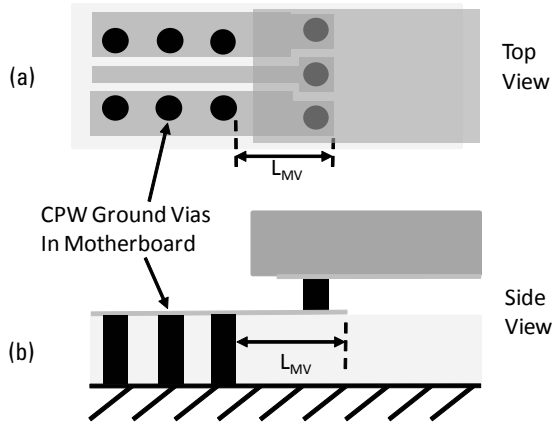


Figure 5.29 A quarter-wave resonance can occur at the flip chip transition if grounding vias are not properly located near the bump pads on the ground path.

where:

f_{MV} = frequency of resonance due to the stub created at the flip chip bump transition

v_0 = free-space velocity

ε_{rMB} = dielectric constant of the motherboard

L_{MV} = the distance between the first motherboard via and the end of bump pad.

Another parasitic effect, though much less common, is a resonance that can be set up around the peripheral bumps of an IC. If the peripheral bumps are connected but not ground properly, a half-wave resonance can be generated between grounded pads. Figure 5.30 illustrates this configuration. For high-gain ICs, resonance can exhibit itself as an oscillation since energy can couple from the output of an amplifier back to its input. This resonant frequency is given by

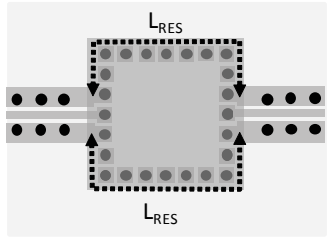


Figure 5.30 Proper grounding of peripheral bumps is required to avoid an undesired resonance.

$$f_{RES} = \frac{v_o / \sqrt{\varepsilon_{rMB}}}{2 L_{MV}} \tag{5.31}$$

where f_{RES} is the resonance due to ungrounded peripheral bumps and pads.

5.3.4 Thermal Concerns for Flip Chips

Face-up ICs have their heat removed through their semiconductor substrate. For example, a traditional face-up MMIC is thinned to approximately 0.1 mm (or 0.05 mm for some high-power MMICs) and the heat generated by the active devices is removed from the bottom of the die. Normally, the bottom of the die is either epoxy attached or eutectic solder attached to a thermal path. Although GaAs is a relatively poor thermal conductor at approximately 45 W/mK, the short thermal path through the thinned die allows for acceptable thermal performance in most cases. Removing the heat from flip chip devices is difficult because the heat removal surface is facing up and the die is full thickness at approximately 0.5 mm so that the thermal resistance will be as much as five times higher for the face-up case. A possible solution to this problem is to use thermal bumps that are grown on the active device so that the heat can be removed directly. In this instance, if a high thermal conductivity substrate such as aluminum nitride is used, the resulting thermal performance can be acceptable for most applications.

Questions

1. What is a first-level interconnect?
2. Derive (5.7) and (5.8).
3. Explain why copper wire bonds require a different IC pad metallization system.
4. What are the benefits of a flip chip IC compared to a conventional face-up IC? What are the disadvantages?
5. Calculate the proximity effect of the motherboard on a flip chip in GaAs with $\varepsilon_r = 12.9$, $W_{IC} = 0.1$ mm, $G_{IC} = 0.07$ mm, $h_{IC} = 0.5$ mm, $h_{MB} = 0.254$ mm, and a motherboard dielectric constant of 9.8. Show the proximity effect by plotting the line impedance and effective dielectric constant as a function of bump height from 0.015 to 0.2 mm.
6. Given that the motherboard material is LTCC ($\varepsilon_r = 5.9$) and a motherboard thickness of 0.254 mm and motherboard metal thickness of 0.0125 mm, for the flip chip configuration shown in Figure 5.29,

determine the transmission line dimensions (W_{MB} and G_{MB}) required to achieve 50Ω and calculate the maximum distance that the first via in the motherboard can be from the flip chip transition.

7. Assuming a straight wire bond exists between two microstrip lines, calculate its inductance if the wire diameter is 0.0254 mm, length is 1.5 mm, and it is 0.5 mm over the ground plane as shown in Figure 5.8.
8. With the same assumption of a straight wire over a ground plane in Question 8, treat the straight wire bond as a transmission line and calculate the line impedance and effective dielectric constant. Plot the insertion loss and return loss of the wire bond using the simple inductive model and the transmission line model from 0.5 to 50 GHz.
9. Calculate the DC resistance of a gold wire with a diameter of 0.05 mm and a length of 1.5 mm.
10. Using an inductive and capacitive section of microstrip line feeding the wire bond, design a matching circuit that will tune out the wire bond inductance of a wire with a diameter of 0.0254 mm and a length of 1.5 mm. Assume the substrates are 0.5-mm-thick alumina with a dielectric constant of 9.8.
11. Name three types of flip chip interconnects.
12. Give a description of the parasitic modes that exist at a flip chip interconnect. Be sure to describe the PPL1 and PPL2 modes.
13. Calculate the frequency of the parasitic resonance caused by the stub created at a flip chip transition given that the motherboard has a dielectric constant of 8.5, a thickness of 0.5 mm, a 50Ω transmission line on the motherboard, and a distance between the first motherboard via and the end of the bump pad of 2 mm.

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6

Second-Level Interconnects

Second-level interconnects exist between the package and the motherboard. Microwave and millimeter-wave application of second-level interconnects is more challenging than for lower frequencies because of the signal transition from the motherboard into the package. If this transition is not carefully designed, its performance of this transition task will dominate the electrical performance of the package. This is true of low-cost, plastic, small outline packages, quad flat no-lead (QFN) packages, packages with leads, solder bump packages, and even the transmission lines that exist in the motherboard. As we will see in this chapter, the electrical performance of second-level microwave packaging is subject to parasitic effects, resonances, coupling, and oscillations.

A small outline package (SOP) is shown in Figure 6.1. Variants of it are the thin small outline package (TSOP) and the thin shrunk small outline package (TSSOP). These packages are surface mounted to a motherboard and they replace the earlier dual inline packages (DIPs) that used through holes in the motherboard for mounting. The SOP and its variants can be made with a thermal pad exposed on the bottom of the package to provide a heat path for power dissipated in the IC. The leads and die paddle are copper that has been plated with a tin finish.

A QFN package is shown in Figure 6.2. It is also a surface-mount package and is used extensively for microwave and millimeter-wave applications. It normally has an exposed thermal pad on the bottom. The reason this package is so popular for rf applications is because the signal path from the motherboard to the wire bond is short. This short path results in less severe parasitic effects and provides wider electrical bandwidth performance.

For the most part, the SOP and plastic QFN encapsulation material are in intimate contact with the surface of the IC. For many applications this is not an issue since the IC is designed to accommodate the effects of the encapsulated

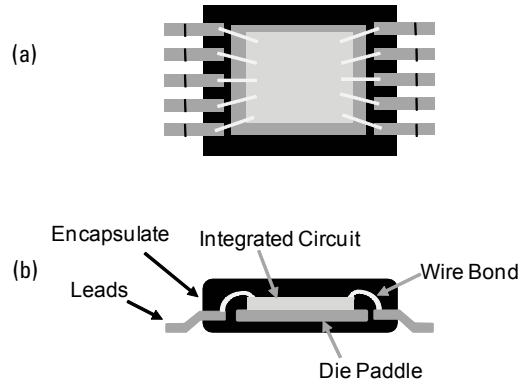

Figure 6.1 Illustration of a small outline package.

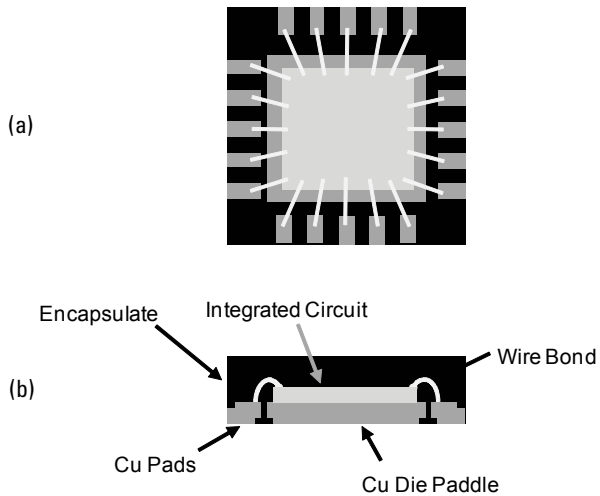

Figure 6.2 Illustration of a QFN package.

material or the effects are minor enough that they can be tolerated. However, for some applications, the IC performance is degraded enough by the encapsulated material that an alternative method must be used.

There are variations on the QFN package such as ceramic versions fabricated in either LTCC or HTCC alumina and liquid crystal polymer (LCP) versions, which utilize an air cavity above the integrated circuit as shown in Figure 6.3. The air cavity allows the IC to avoid intimate contact with an encapsulated material on its surface. To understand why contact between the encapsulate and IC is undesirable, consider the graph in Figure 6.4. It shows the impedance change for a transmission line on a 0.101-mm-thick GaAs MMIC when an encapsulated material is placed over it. Most encapsulated materials have a

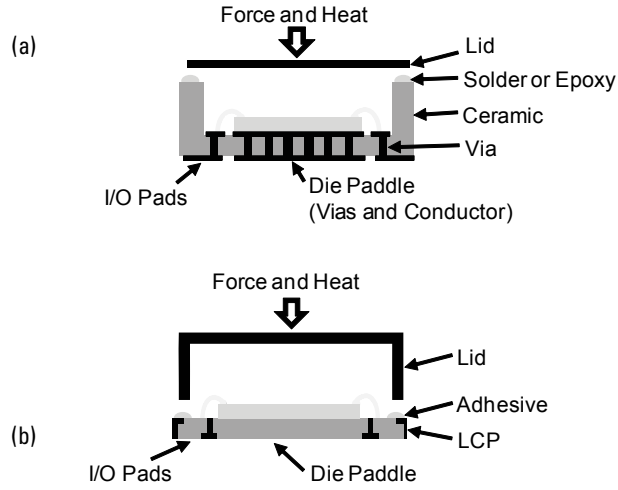

Figure 6.3 Illustration of air cavity packages realized using (a) a ceramic QFN package with side walls or (b) an LCP base with an LCP lid.

dielectric constant between 2.5 and 5, so the figure shows the line impedance with air over the MMIC transmission line and with dielectric constants of 3 and 5 as a function of the width of the transmission line. The figure also shows the impact of encapsulate on the effective dielectric constant of the microstrip line. The results show that that impedance for a 0.0254-mm line changes by 7Ω and the effective dielectric constant varies by 1.76 when an encapsulate with a dielectric constant of 5 is added over the MMIC. The impact on the performance of the IC will vary depending on the type of integrated circuit, and the effect can actually be accounted for in the design of the MMIC.

In addition to transmission line impedance and effective dielectric constant shifts, encapsulated material will cause insertion loss of the signal. The effects of glob top, which is a type of encapsulate, on the transmission characteristics of CPW lines have been studied by Baumann et. al. [1]. They found that the presence of the encapsulate caused an 11% decrease in line impedance and a 12% increase in phase constant and attenuation. The researchers also found that CPW transmission line loss increased by 0.6 dB/cm due to the presence of the encapsulate material over the transmission line.

Encapsulation of microwave and millimeter-wave circuits resulting in a surface-mountable package has been demonstrated using LCP [2]. A CMOS power amplifier operating at 90 GHz was packaged using an air cavity and flip chip attachment using stud bumps. This demonstrates the usefulness of surface-mount packages for the realization of millimeter-wave packaged ICs. However, proper electrical modeling is required, as discussed next.

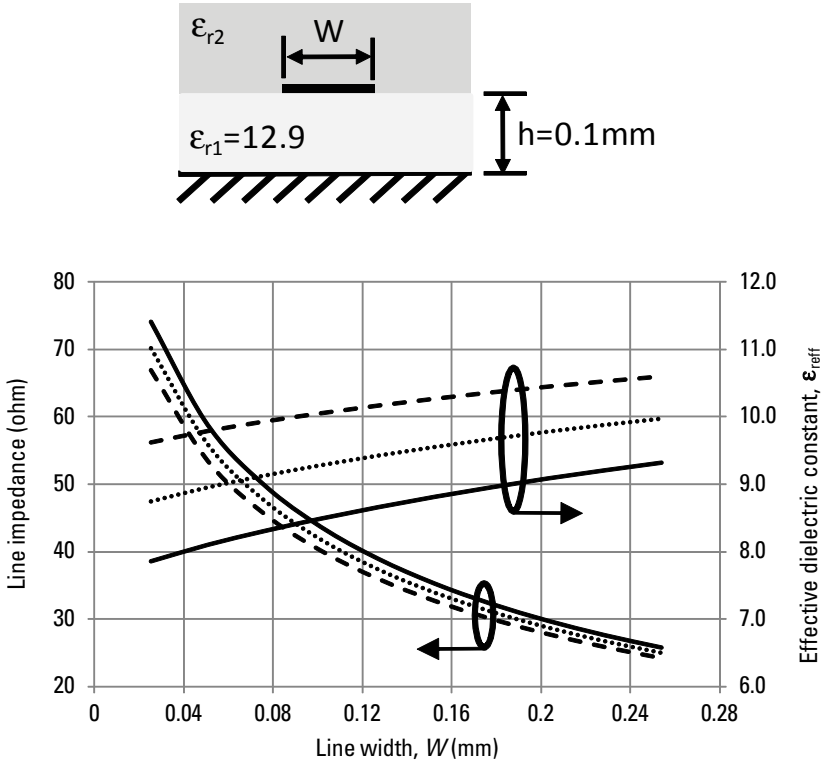

Figure 6.4 The effect of an encapsulate over a GaAs MMIC transmission line is that it lowers the impedance of the line. (Note: Solid line is for air with $\varepsilon_{r2} = 1$; dotted line is for $\varepsilon_{r2} = 3$; and dashed line is for $\varepsilon_{r2} = 5$).

6.1 Electrical Modeling of Surface-Mount Packages

The task of electrical modeling of surface-mount packages at microwave and millimeter-wave frequencies presents the challenge of accounting for effects in the motherboard and the package transition. Most diligent designers will extend the analysis to include the wire bond so that they can optimize all of the effects from the transmission line on the motherboard all the way up to the bond pads on the IC. In practice, most designers use EM simulators to analyze and optimize the packaging interconnect or measured data on the package. Usually, the simulation results are imported into circuit simulators. For transient and time domain simulations, it is best to use equivalent circuits such as inductors, capacitors, and resistors. Therefore, many designs require the development of an equivalent circuit that matches the results from the EM simulator or measured data. Several methods have been developed to model the effect.

6.2 Inductance and Capacitance Matrix Method for Package Model Extraction

A method for package modeling was developed Brian Young and Aubrey Sparkman that uses scattering parameters to calculate the parameters of an equivalent circuit [3]. The benefit of a vector network analyzer (VNA) is that high-precision coaxial probes can be used to very accurately measure the scattering parameters of the package, which cannot be achieved using simple voltage and current probes. The resulting scattering parameters can be used to calculate the LCR matrix that describes the package electrical interconnects. Consider Figure 6.5, which shows the equivalent LCR circuit that describes the operation of the package. From Kirchhoff's voltage law, we find

$$\bar{V}^L - \bar{V}^R = \left(\mathbf{R} + j\omega\mathbf{L}\right)\bar{I}^L \tag{6.1}$$

and from Kirchhoff's current law

$$\bar{I}^R + \bar{I}^L = \left(\mathbf{G} + j\omega\mathbf{C}\right)\bar{V}^R \tag{6.2}$$

where $\bar{V}^L, \bar{V}^R, \bar{I}^L$, and $\bar{I}^R$ are defined in Figure 6.5 and:

L = inductance matrix
C = capacitance matrix
R = resistance matrix.

Equations (6.1) and (6.2) fully describe the package over the bandwidth for which the equivalent circuit in Figure 6.5 is valid. Now, we must develop a

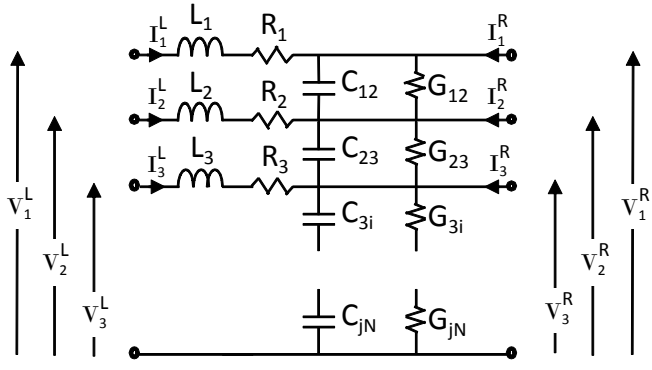

Figure 6.5 Circuit elements of the inductance and capacitance matrix model simplified for clarity. (From: [3]. ©1996 IEEE. Reprinted with permission.)

procedure for determining the matrices' LCR. One method is to recognize that if $\overline{V}^R = 0$, which means that pins are shorted to ground at the interior to the package, then (6.1) becomes

$$\overline{V}^L = \left(\mathbf{R} + j\omega\mathbf{L}\right)\overline{I}^L \tag{6.3}$$

If a one-port measurement is taken at Port 1 of the VNA on the mth line with all pins of the package shorted so that $\overline{V}^R = 0$ on them, then (6.3) becomes

$$v_1 = \left(R + j\omega L\right)_{mm} i_1 \tag{6.4}$$

At this point in the derivation, a slight detour is required to introduce the useful notation of forward and reverse traveling waves for a multiport device. Consider the *n*-port shown in Figure 6.6. Note that the port voltages v_1, v_2, …, v_n are composed of forward and reverse traveling waves. Forward traveling waves entering the port are noted by V_n^+ and reverse traveling waves leaving Port V_n^- where *n* is the Port number. Measurement conducted using a VNA will capture forward and reverse waves as part of the information in the scattering parameters [4, 5]. For a two-port device, the port voltages and currents are given by

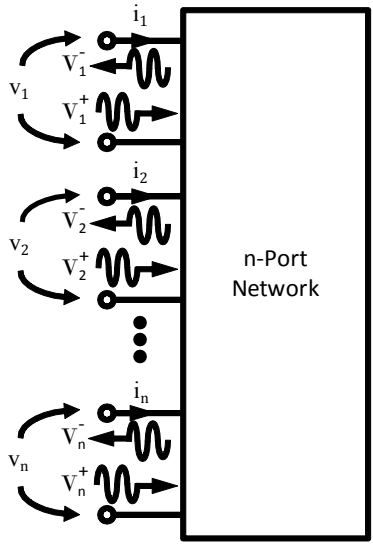

Figure 6.6 Port voltages and currents for an n-port network showing the forward (V_n^+) and reverse (V_n^- traveling waves at the nth port.

$$v_1 = V_1^+ + V_1^- \tag{6.5}$$

$$v_2 = V_2^+ + V_2^- \tag{6.6}$$

$$i_1 = \frac{1}{Z_o}\left(V_1^+ + V_1^-\right) \tag{6.7}$$

$$i_2 = \frac{1}{Z_o}\left(V_2^+ + V_2^-\right) \tag{6.8}$$

where:

v_1, i_1 and v_2, i_2 = voltage and current, respectively, measured at Port 1 and Port 2 of a VNA

V_1^+, V_1^- and V_2^+, V_2^- = forward and reverse waves, respectively, measured at Port 1 and Port 2 of a VNA

Z_0 = the characteristic impedance of the VNA measurement system (usually 50Ω).

Now, returning to the derivation, we can plug (6.5) and (6.7) into (6.4) and use the fact that S11 = *V*–/*V*+ to obtain

$$\left(\mathbf{R} + j\omega\mathbf{L}\right)_{mm} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{6.9}$$

which allows the calculation of the diagonal terms of the matrices to be determined.

If two port measurements are conducted such that Port 1 of the VNA is connected to the *m*th line and Port 2 of the VNA is connected to the *n*th line, with all other ports short circuited, then (6.3) simplifies to

$$v_1 = \left(R + j\omega L\right)_{mm} i_1 + \left(R + j\omega L\right)_{mm} i_2 \tag{6.10}$$

where is the current measured at Port 2 of the VNA.

By substituting the traveling-wave relationships (6.5) and (6.8), by recognizing that $V_1^+ = 0$ since Port 1 is impedance matched and that $S12 = V_1^- / V_2^+$ and by substituting (6.9), we obtain

$$\left(\boldsymbol{R}+j\omega\boldsymbol{L}\right)_{mn}=\left[Z_0+\left(\boldsymbol{R}+j\omega\boldsymbol{L}\right)_{mm}\right]\frac{S_{12}}{1+S_{22}} \tag{6.11}$$

Note that $(R + j\omega L)$mm is given by (6.9) so that (6.11) can be calculated. The result of (6.9) and (6.11) is that the resistance and inductance matrices can be filled out.

The capacitance and conductance matrices can be determined by following a similar procedure. If the pins on the package are open circuited so that $\overline{I}^{L} = 0$, then (6.2) simplifies to

$$\overline{V}^{R}=\left(\mathbf{G}+j\omega\mathbf{C}\right)^{-1}\overline{I}^{R} \tag{6.12}$$

The same procedure can be followed as for the short circuit case so that

$$\left(\mathbf{G}+j\omega\mathbf{C}\right)^{-1}_{mm}=Z_0\frac{1+S_{11}}{1-S_{11}} \tag{6.13}$$

$$\left(\boldsymbol{G}+j\omega\boldsymbol{C}\right)^{-1}_{mn}=\left[Z_0+\left(\mathbf{G}+j\omega\mathbf{C}\right)^{-1}_{\mathrm{mm}}\right]\frac{S_{12}}{1+S_{22}} \tag{6.14}$$

Note that (6.13) and (6.14) yield the inverted conductance and capacitance matrix so that by matrix inversion (**G** + jωC) can be obtained.

A test plan for implementing this method is to prepare two samples: one with all pins shorted to the die paddle and the other with all pins not shorted to the die paddle, but left open circuited. The packages can then be mounted to a motherboard that shorts the die paddle to the reference level (ground in most cases) and then the one-port and two-port measurements are conducted. This configuration is shown in Figure 6.7.

This is a very powerful method that can be used to extract the inductance and capacitance of electronic packages. A few important observations should be made about his method:

- This method can be applied to very high lead count packages.
- As the number of leads increases, the coupling to distant pins decreases so that the actual number of measurements required is reduced.
- This method assumes that the ground point for each measurement is the same. In other words, it assumes that there is zero ground inductance between the measurement points for every measurement. This is clearly

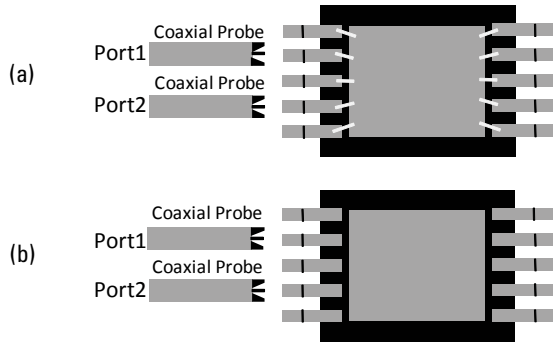

Figure 6.7 The LCR matrix method uses two test configurations: (a) one with all of the pins shorted to the die paddle to extract the R and L matrices and (b) one with all of the pins floating to extract the G and C matrices. (From: [3]. ©1996 IEEE. Reprinted with permission.)

not the case for nonadjacent pins so that some measurement error is introduced, and the error increases as the distance between measured pins increases. However, it has been shown that the effect of the inductive return path is not a significant contributor to the error in measurement [6].

The frequency range over which this method is appropriate depends on the ability of the LCR model in Figure 6.5 to capture the parasitic effects of the package.

This method has been applied to a 5-mm × 5-mm QFN package with pin pitch of 0.65 mm and pin width of 0.35 mm. In this analysis the package is assumed to be excited on one side of the package by adjacent signals that are separated by ground. The model used for the HFSS simulations is shown in Figure 6.8. A simplified model using only the diagonal elements of the matrix for the calculations is shown in Figure 6.9. It is possible to automate the calculation of (6.9) and (6.13) within a circuit simulator to automatically extract the equivalent circuit model. This was done and the element values calculated at 5 GHz are shown in Table 6.1. Figure 6.10 shows a comparison of the EM simulator and circuit simulation results.

Although a simplified version of the model has been used in this analysis, a more rigorous implementation is possible.

6.3 Coupled-π Model Method

The coupled-π model method uses inductors with magnetic coupling and capacitive elements as the equivalent circuit model [7–9]. The model elements can be calculated from measured data or EM simulator scattering parameters.

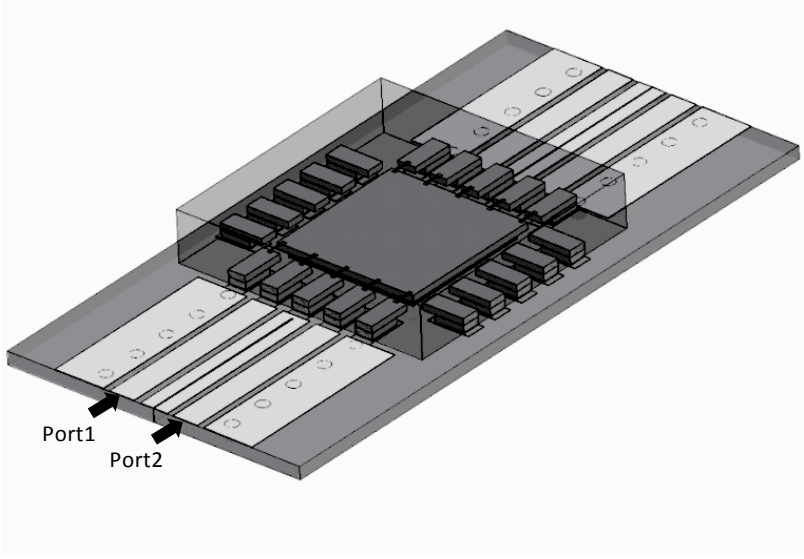

Figure 6.8 HFSS model of a 5-mm 5-mm QFN package with 0.65-mm pin pitch and 0.35-mm-wide pins.

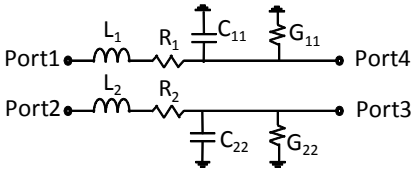

Figure 6.9 Simplified model of the 5-mm × 5-mm QFN package using the LCR matrix method.

Table 6.1
Model Element Values Calculated Using (6.9) and (6.13)

Model Element	Calculated Value
L1 = L2	0.5722 nH
R1 = R2	0.0434Ω
C11 = C22	0.17 pF
G11 = G22	7.74×10^{-6}

The procedure for implementing the coupled-π model is essentially the same as that used for the LC matrix method. Package samples are either prepared for measurement or models are generated for EM simulation. Two-port

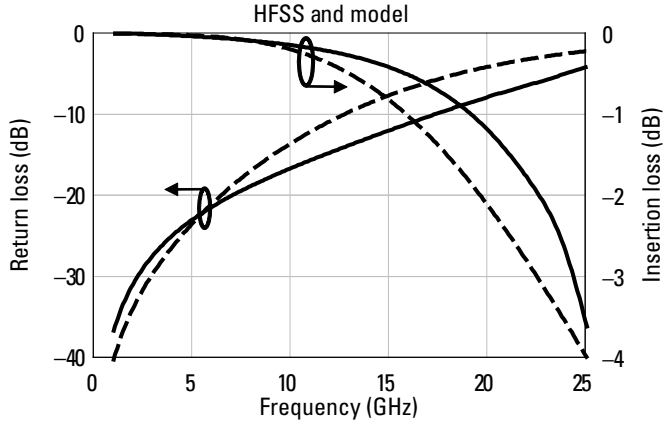

Figure 6.10 Comparison of the EM simulator return loss and insertion loss results for the QFN package shown in Figure 6.8 with the equivalent model in Figure 6.9 using the element values listed in Table 6.1. (Note: Solid curve = EM simulator result; dashed curve = equivalent model result.)

scattering parameters are measured for either case with the leads shorted or open as illustrated in Figure 6.7 to generate open-circuit-path (op) and short-circuit-path (sp) scattering parameters. The scattering parameters are used to calculate the equivalent circuit element values.

The schematic for the interconnect equivalent model is shown in Figure 6.11 for two leads of a package. It shows the series inductance L_i and shunt capacitance C_i, which account for the package lead inductance and ground capacitance, respectively. Note that C_i includes the parasitic capacitances and the capacitance from the package lead to the motherboard ground plane. The mutual inductance M_{ij} and mutual capacitance C_{ij} account for the coupling between the two package leads.

The values of the equivalent circuit elements can be approximated [7] using

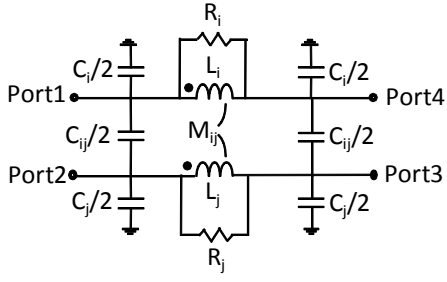

Figure 6.11 Schematic of the coupled-π model of the package interconnect.

$$C_{i,j} \sim \frac{-\tan\left(\text{ang}\left(S_{11}^{op}/2\right)\right)}{2\pi f Z_0} - C_{ij} \tag{6.15}$$

$$C_{ij} \sim \frac{1}{4\pi f Z_0} \frac{\left|S_{21}^{op}\right|}{\sqrt{1-\left|S_{21}^{op}\right|^2}} \tag{6.16}$$

$$L_{i,j} \sim \frac{Z_0}{2\pi f} \cot\left(\frac{\text{ang}(S_{11}^{SP})}{2}\right) \tag{6.17}$$

$$L_{i,j} \sim \frac{Z_0}{2\pi f} \cot\left(\frac{\text{ang}(S_{11}^{SP})}{2}\right) \tag{6.18}$$

where:

$C_{i,j}$ = capacitance to ground for package lead i and j
C_{ij} = mutual capacitance between package lead i and j
$L_{i,j}$ = lead inductance for package lead i and j
M_{ij} = mutual inductance between package lead i and j
S_{11}^{op} = S11 scattering parameter from the open-circuit-path easurements
S_{12}^{op} = S21 scattering parameter from the open-circuit-path measurements
Z_0 = impedance of the VNA measurement system
f= frequency at which the VNA measurement is conducted.

Because many circuit simulators use the coupling coefficient between coupled inductors rather than mutual coupling, it is convenient to use

$$K_{ij} = \frac{M_{ij}}{\sqrt{L_i l_J}} \tag{6.19}$$

The HFSS simulation results for the QFN model in Figure 6.8 were compared to the equivalent circuit model in Figure 6.11. Recall that Figure 6.8 shows a 5-mm × 5-mm QFN package with a pin pitch of 0.65 mm and pin width of 0.35 mm. Figure 6.12 shows the results of the comparison. The

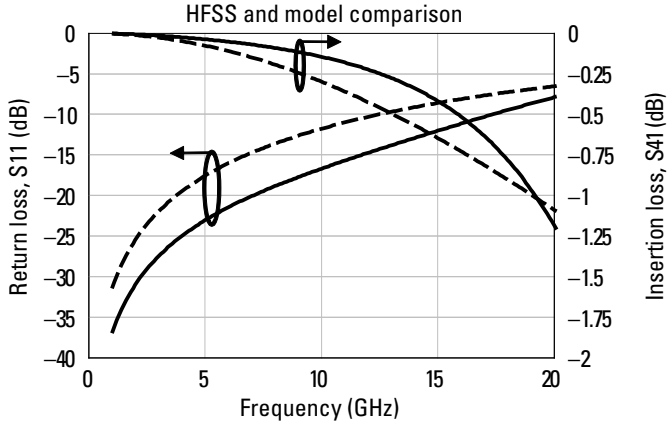

Figure 6.12 Comparison of the EM simulator return loss and insertion loss results for the QFN package shown in Figure 6.8 with the equivalent model in Figure 6.11 using the element values listed in Table 6.2. (Note: Solid curve = EM simulator result; dashed curve = equivalent model result.)

agreement between the measured and modeled insertion loss and return loss can be improved. The calculated values of the model elements are shown in Table 6.2.

The model can be improved by optimizing the value of C12. If C12 is optimized to –0.031 pF and its magnitude is subtracted as directed by (6.15), then significantly better agreement is achieved for the return loss and insertion loss as shown in Figure 6.13. Also, the agreement for isolation is excellent for optimized values of C12 as shown in Figure 6.14. The optimized model values are shown in Table 6.3.

The benefit of this modeling method is that calculation of the element values is straightforward and, with some minor optimization, an accurate match between measurements and the model can be achieved for the magnitude of the scattering parameters to 20 GHz. A drawback to this method is that

Table 6.2
Model Element Values
Calculated Using (6.5) to (6.19)

Model Element	Calculated Value
C1	0.169 pF
C12	0.00091 pF
L1	0.666 nH
M	0.00227
K	0.0034

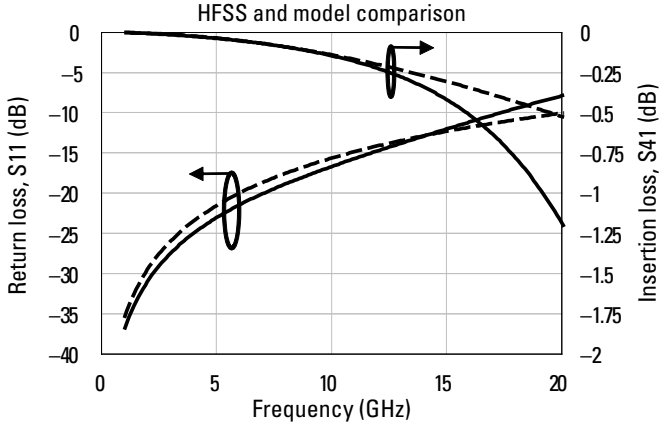

Figure 6.13 Comparison of the EM simulator return loss and insertion loss results for the QFN package shown in Figure 6.8 with the equivalent model in Figure 6.11 using the element values listed in Table 6.3. (Note: Solid curve = EM simulator result; dashed curve = equivalent model result.)

Table 6.3
Model Element Values Calculated Using (6.5) to (6.19) with the Value of C12 Optimized

Model Element	Calculated Value
C1	0.138 pF
C12	–0.031 pF
L1	0.666 nH
M	0.00227
K	0.0034

the phase delay through the interconnect is not accurately predicted. Figure 6.15 shows the insertion phase of the model versus the insertion phase of the HFSS model. Note the error in the simulation. This error can be corrected by using a transmission line in the model as shown in Figure 6.16. The length of the transmission line was optimized to be 1.07 mm with a line impedance of 50Ω and an effective dielectric constant of 3. Figure 6.17 shows the improved match between the HFSS and equivalent model phase after these adjustments.

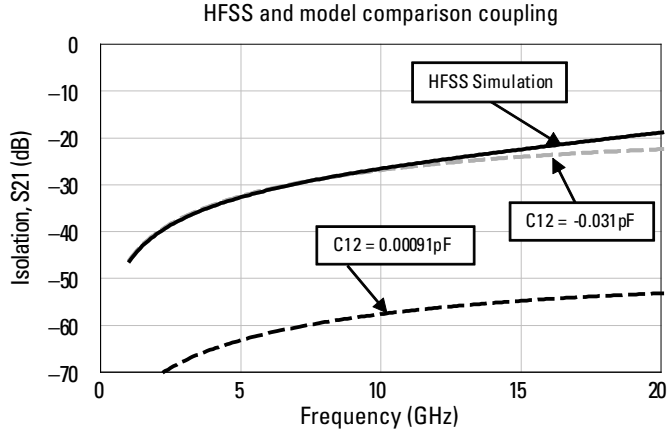

Figure 6.14 Comparison of the EM simulator isolation results for the QFN package shown in Figure 6.8 with the equivalent model in Figure 6.11 using the element values listed in Table 6.3. (Note: Solid curve = EM simulator result; dashed curve = equivalent model result.)

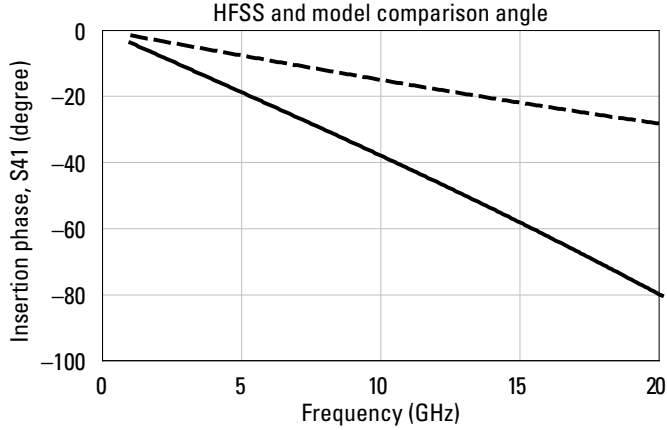

Figure 6.15 Comparison of the EM simulator insertion phase results for the QFN package shown in Figure 6.8 with the equivalent model in Figure 6.11 using the element values listed in Table 6.3. (Note: Solid curve = EM simulator result; dashed curve = equivalent model result.)

6.4 Hybrid Circuit Model

An improved modeling method for second-level interconnects appropriate for capturing electrical performance into the millimeter-wave range is the hybrid circuit model method. In this approach, a combination of lumped elements and transmission lines is used to model the package. The procedure is less capable of

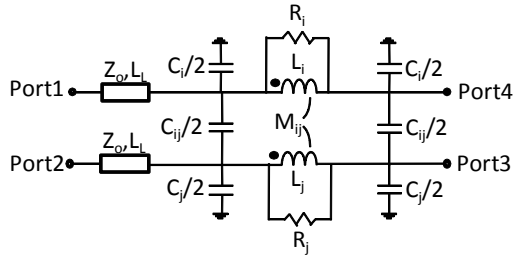

Figure 6.16 The equivalent model from Figure 6.11 modified to include an input line length that accounts for the phase delay through the interconnect.

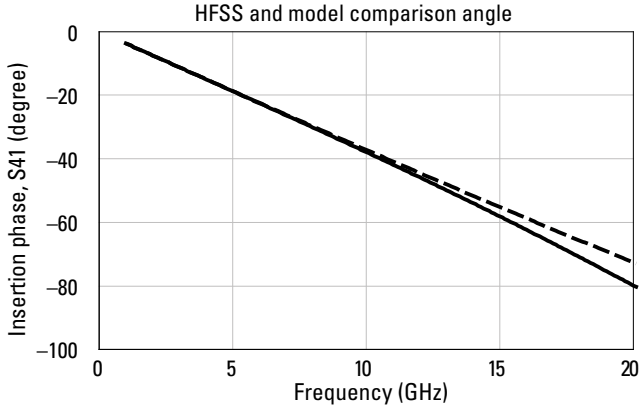

Figure 6.17 Comparison of the EM simulator insertion phase results for the QFN package shown in Figure 6.8 with the equivalent model in Figure 6.16 using the element values listed in Table 6.3 and a 1.07-mm line with 50Ω impedance and an effective dielectric constant of 3. (Note: Solid curve = EM simulator result; dashed curve = equivalent model result.)

automation compared to the coupled-π method and the LCR matrix method; however, it is much more accurate in the millimeter-wave range.

The basis of the model is that the package's physical features are modeled as transmission lines. This method requires insight from the designer so that those sections of the package interconnect that behave as transmission lines can be identified. Some implementations of this method used de-embedding methods, which systematically allow access to portions of the circuit that are "buried" within the package interconnect [10].

This method has also been applied successfully to ball grid array (BGA) packages using coplanar waveguide transmission line models for the transmission lines and an LC network for the ball interconnect. This method achieved good agreement between measured and modeled performance for an 8-GHz package [11] and also for a 36-GHz package [12].

The hybrid model method was applied for the measurement of a shrunk small outline package (SSOP), which was successfully characterized to 26.5 GHz [13]. A variation of this method was used to measure the performance of a QFN package to 40 GHz [14].

Questions

1. What is a second-level interconnect? Contrast and discuss the differences with first-level interconnects.
2. What are the differences and/or similarities between SOP, TSOP, TSSOP, QFN, and DIP packages? Are DIP packages useful for millimeter-wave frequencies and why?
3. Show the detailed derivations of (6.9) and (6.11).
4. Show the detailed derivations of (6.13) and (6.14).
5. Calculate the package equivalent circuit model using the LCR matrix method for a package with the follow scattering parameters for the open and short circuit case (assume the circuit is reciprocal):

Case	Freq (GHz)	S_{11} Mag	S_{11} Ang	S_{21} Mag	S_{21} Ang
Open	1.0	.9998	–5.946	0.00074	84.018
Short	1.0	0.9995	170.86	0.00178	80.141

6. Calculate the package equivalent circuit model using the coupled-π method for a package with the same scattering parameters as Question 5.

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7

Modules and Motherboards

Microwave modules have traditionally been hermetic metal "boxes" with microelectronic assemblies containing bare die ICs and wire bonds to connecting transmission lines. Although this type of module is still used extensively, it is being replaced by laminate motherboards with solder-attached, surface-mount technology (SMT) QFN-style packages with microwave and millimeter-wave ICs in them. These features and others result in modules and laminate motherboards at rf frequencies that have challenges that are not present in DC or low-frequency applications. This chapter considers these unique challenges for both microelectronic hybrids and motherboards.

It may seem curious that microwave hybrids and motherboards are being discussed in the same chapter. This approach is reasonable because of the commonalities that exist between them. As already pointed out, most microwave hybrids (microelectronic assemblies) consist of ICs (in bare die form) mounted onto a substrate and interconnected by transmission lines. The electrical design concerns for this type of module are transmission line design, coupling between transmission lines, resonances in the module, and transitions between different planar transmission line types.

This is similar to a laminate motherboard with SMT-attached microwave or millimeter-wave ICs in packages. The SMT packages are interconnected with transmission lines. The electrical design concerns are the same as for the microelectronic hybrid module. This is especially true for motherboards with metal shields, which can appear electrically as resonant cavities and result in the same type of resonances that occur with a hybrid module. Therefore, this chapter focuses on the electrical design issues that both microwave hybrids and microwave PCB motherboards share.

7.1 Proper Transmission Line Design

Several aspects must be considered when designing transmission lines. The most obvious is choosing the dimensions and materials so that the desired line impedance and low-loss signal propagation are realized. Line impedance calculations are straightforward using closed-form equations or a commercially available transmission line calculator. Other concerns are undesired resonances and higher order mode generation. In this section we consider the proper design of a few transmission line types.

7.1.1 Conductor-Backed Coplanar Waveguide

Coplanar waveguide (CPW) transmission lines, illustrated in Figure 7.1(a), have been used for many applications including filters, MMICs, and packaging [1–3]. For packaging in modules and motherboards, the vast majority of practical applications require the use of a ground plane under the CPW line. Once a lower ground plane is added, a CPW is properly called a conductor-backed coplanar waveguide (CBCPW) and is illustrated in Figure 7.1(b).

CBCPW lines have become extremely popular for modules and motherboards. This is due to the fact that it offers easy access to a ground connection because the ground plane is on the same level as, and very close to, the signal line (which is not the case for most other transmission lines). In addition, a CBCPW has lower dispersion than a microstrip, which makes it popular for wideband systems such as optical telecom modules and motherboards that must work over bandwidths of 10 to 100 GHz or more. Also, the backside ground plane allows the substrate to be connected to a heat sink. It permits the introduction of ground areas on the topside of the substrate to improve isolation. It

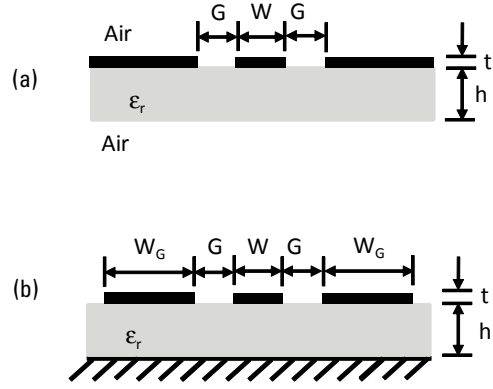

Figure 7.1 Comparison of (a) a coplanar waveguide and (b) a conductor-backed coplanar waveguide.

also can improve mechanical strength when the ground plane is connected to a support structure and it improves the ability to transition to other transmission lines such as microstrip lines. One drawback is that it has a higher insertion loss per unit length than microstrip lines since it uses a slot-type mode for propagation, which results in higher current density near the edges of the signal line. Our analysis of CBCPW will initially focus on the proper design of the transmission line to achieve the desired line impedance, and then focus will shift to understanding some of the undesired effects such as parasitic modes.

The design equations for the line impedance and effective dielectric constant for CBCPW can be obtained using conformal mapping techniques [4, 5]. Referring to Figure 7.1(b) for the definition of the dimensions, the effective dielectric constant and line impedance, assuming that W_G is large compared to $W+ G$, are given by

$$\varepsilon_{reff} = \frac{1 + \varepsilon_r \dfrac{K(k')}{K(k)} \dfrac{K(k_3)}{K\left(k_3^{'}\right)}}{1 + \dfrac{K(k')}{K(k)} \dfrac{K(k_3)}{K(k_3')}} \tag{7.1}$$

$$Z_0 = \frac{60\pi}{\sqrt{\varepsilon_{reff}}} \frac{1}{\dfrac{K(k)}{K(k')} + \dfrac{K(k_3)}{K(k_3')}} \quad \text{ohm} \tag{7.2}$$

where:

$k = a/b$

$k_3 = \tanh(\pi a/2h)/\tanh(\pi b/2h)$

$k' = \sqrt{1 - \mathrm{k}^2}$

$k_3' = \sqrt{1 - k_3^2}$

$a = W/2$

$b = W/2 + G$

$K(k)$ = complete elliptical integral of the first kind.

Computation of (7.1) and (7.2) is straightforward using standard closed-form approximations for the complete elliptical integral of the first kind.

The thickness of the transmission line metal impacts the calculation of line impedance and effective dielectric constant. The thickness of the transmission

line metal increases the line capacitance because there is a larger area of metal between the center conductor and topside grounds. Since the line impedance Z0, is equal to $\sqrt{L/C}$ where L and C are the line inductance and line capacitance, an increase in C will cause the line impedance to be reduced. A correction factor, Δ_{CPW}, can be applied to (7.1) and (7.2) to account for the transmission line metal thickness. The correction is achieved by offsetting the line width by $+\Delta_{CPW}$ and gap by the factor $-\Delta_{CPW}/2$, which is given by [6]

$$\Delta_{CPW} = 1.25t\frac{\left[1+\ln(2/t)\right]}{\pi} \tag{7.3}$$

The resulting effective dielectric constant and line impedance are compared to results from HFSS in Figure 7.2. Note that the line impedance predicted by HFSS is slightly lower than is calculated using (7.1) through (7.3). The same is true for the effective dielectric constant.

In addition to properly designing CBCPWs to achieve the required line impedance and effective dielectric constant, it is important to avoid some of the parasitic effects such as undesired modes. Although relatively simple to overcome with proper design practice, CBCPW technology suffers from the

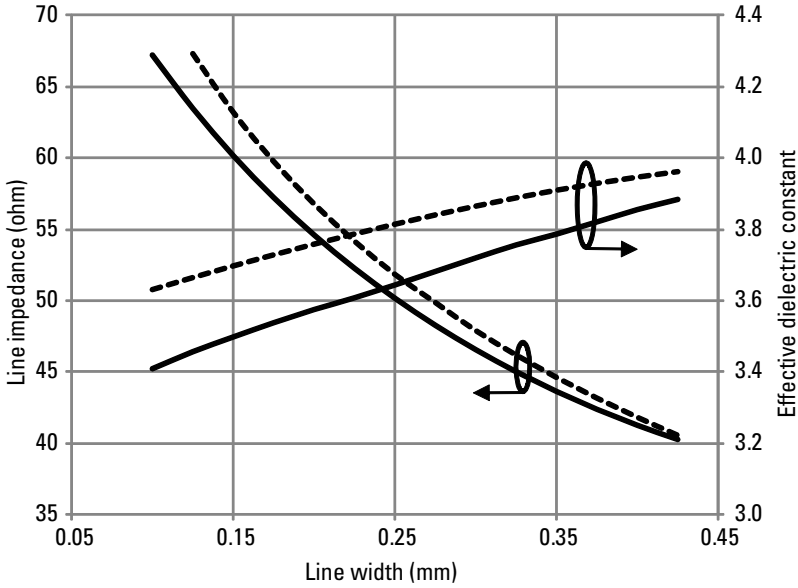

Figure 7.2 Comparison of the line impedance and effective dielectric constant using predictions from HFSS and calculations using (7.1) through (7.3) for $\varepsilon r = 6$, h = 0.254 mm, t = 12.5 μm, and G = 0.125 mm. (Note: Solid lines = HFSS results; dashed lines = calculations.)

fact that it can support three fundamental modes [7–9]. The three dominant modes, one desired mode and two parasitic modes, are shown in Figure 7.3. The desired CBCPW mode, shown in Figure 7.3(a), has field lines emanating from the center conductor to the topside and bottom side ground. As a result, ground currents exist on the topside grounds as well as on the bottom side ground. (Note that the topside grounds and the bottom side grounds are at the same potential.)

One of the undesired modes is the slot line mode as illustrated in Figure 7.3(b). For this mode the topside grounds are at different potentials. This mode can be controlled by using air bridges to connect the topside grounds to the same potential or, even better, by using vias to connect the topside grounds to the bottom side ground.

The other undesired mode is the parallel plate mode, as illustrated in Figure 7.3(c). For this mode, all three topside conductors are at the same potential with field lines emanating to the bottom side ground plane. This mode can also be controlled by using vias connecting the topside grounds to the bottom side grounds. The undesired modes, if not controlled, can result in coupling to

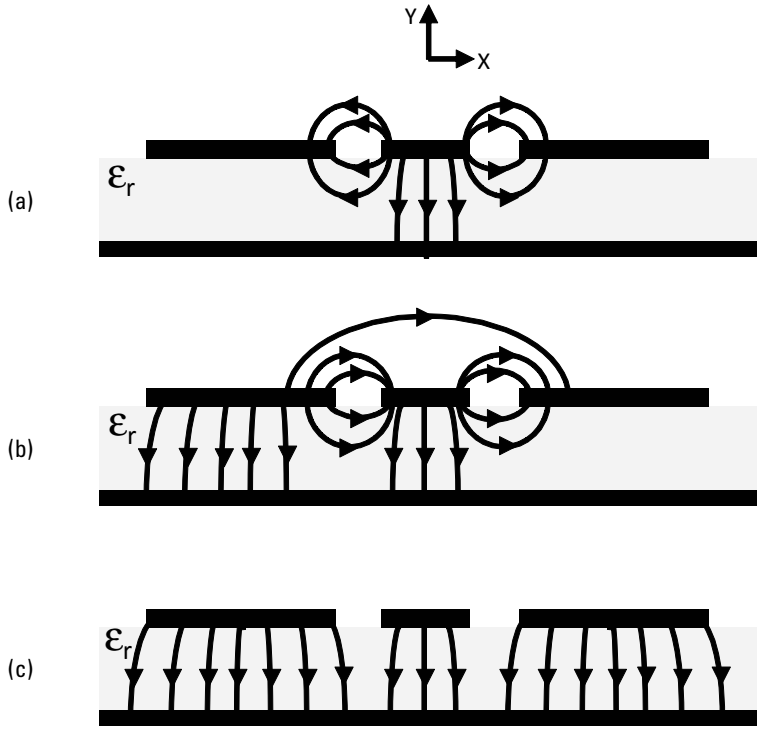

Figure 7.3 The three dominant modes that can exist in CBCPWs: (a) desired mode, (b) undesired slot mode, and (c) undesired parallel plate mode.

other circuits [10]. An excellent treatment of the fundamental and higher order modes in CBCPW can be found in Refs. [11–13]. Energy will be coupled from the desired mode to undesired modes at discontinuities or transitions and also through leakage. Though the existence of these undesired modes is important to consider in the design of CBCPWs, in practical terms, they are normally controlled by using vias connecting the topside and bottom side grounds.

In addition to the three fundamental modes, there are modes that can be supported along the length of the transmission line, which, if not controlled, result in resonances [14, 15]. Figure 7.4 illustrates a CBCPW transmission line with topside ground metal, a center conductor width of W_G, and a line length of L_G. Without vias, these patches of topside ground metal will create insertion loss resonances that will render the transmission line useless at and above the frequency where the resonances begin to occur. The resonant frequencies can be modeled as rectangular patch antennas with resonant frequencies give by

$$f_{mn} = \frac{v_0}{2\sqrt{\varepsilon_r}} \sqrt{\left(\frac{m}{W_G}\right)^2 + \left(\frac{n}{L_G}\right)^2} \quad \text{Hz} \tag{7.4}$$

where:

v_0 = speed of light in a vacuum

ε_r = dielectric constant of the substrate

W_G = width of the topside ground

L_G = length of topside ground without grounding vias (when vias are used instead of L_G, use D_P, which is the pitch between vias)

m, n = indices for the resonant modes.

For the case of no vias on the CBCPW topside ground, (7.4) is useful in predicting the resonant behavior. Method of moment (MoM) using EMSight

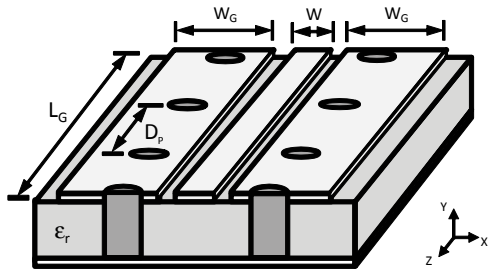

Figure 7.4 CBCPW with ground vias at a pitch of DP connecting the topside ground metal, which is WG wide and LG long, to the bottom side ground metal.

and HFSS simulations were conducted to determine the first few resonant modes for comparison to (7.4). The first resonant mode is the most important since it determines the highest frequency of operation. Table 7.1 summarizes the results. Note that for the structure chosen, the first resonant mode is f_{01}. The table shows that the agreement between resonances calculated by (7.4) and simulated by HFSS agree to within approximately 2.7% or better.

The design of CBCPW transmission lines is not as straightforward as other transmission lines. However, as we have shown by using a few simple design guidelines, it is possible to achieve wide bandwidth performance using CBCPWs. The design guidelines are as follows:

1. Use either the closed-form design equations that were presented or commercially available software for the design of the transmission lines to achieve the desired line impedance.
2. The transmission line will support three modes: the desired CBCPW mode, the slot-like mode, and the parallel plate (also called the microstrip-like) mode. It is important to use vias to connect the topside grounds to the bottom side grounds to inhibit the excitation of these modes.
3. Proper placement of vias connecting the topside ground to the bottom side ground is critical to achieve the bandwidth required. The pitch D_P of the vias should be chosen to avoid the onset of a patch antenna–type mode that resonates along the length of the line. In general, place the vias as close as is allowed by the design rules of the circuit board process. However, as a good rule of thumb, place the vias no more than a quarter wavelength away, which is half the distance that is predicted by (7.4) with L_G replaced by D_P.
4. Use multiple vias on the topside ground at the edge near the gap and the outside edge of the top metal.

Table 7.1
Comparison of (7.4) and HFSS for the Prediction of Resonant Modes on the Topside Ground Plane of CBCPW, Referring to Figures 7.1 and 7.4 (with $\varepsilon_r = 6.0$, $h = 0.2$ mm, $W_G = 1.016$ mm, $L_G = 5.03$ mm, $W = 0.203$ mm, $G = 0.152$ mm)

Mode Index		Resonant Frequency		
m	n	From (7.4) (GHz)	Simulated HFSS (GHz)	Simulated MoM (GHz)
0	1	12.17	12.5	12.9
0	2	24.35	24.55	25.46
0	3	36.52	36.55	37.74

7.1.2 Striplines

Stripline is a commonly used transmission line when signals need to be routed in buried layers of a ceramic or laminate board. Figure 7.5 illustrates a stripline transmission line. The line impedance of a stripline with $t = 0$ is given by [16]

$$Z_0\sqrt{\varepsilon_r} = 30\pi\frac{K'(k_s)}{K(k_s)} = 30\pi\frac{K(k_s')}{K(k)} \quad \text{ohm} \tag{7.5}$$

where $k_s = \tanh(\pi Ws/2b)$ and

$$k_s' = \sqrt{1-k_s^2}$$

Commercially available software allows for convenient calculation of the line impedance of striplines with or without the thickness of the signal line taken into account. Figure 7.6(a) shows the approximate electric field distribution for a properly designed stripline circuit. Notice how the field lines exist between the strip and the upper and lower ground plane. Very little coupling exists to the vias on either side of the strip.

Striplines can support high-order parasitic modes. If these modes are allowed to propagate, the desired TEM mode will couple most of its energy into these undesired parasitic modes. The effect will be resonant effects. The approximate field distribution for the first parasitic mode is shown in Figure 7.6(b). It is the familiar TE_{01} dielectric loaded waveguide mode. It can propagate if the distance between vias, *a*, is too large. The resonant frequency of that mode is given by

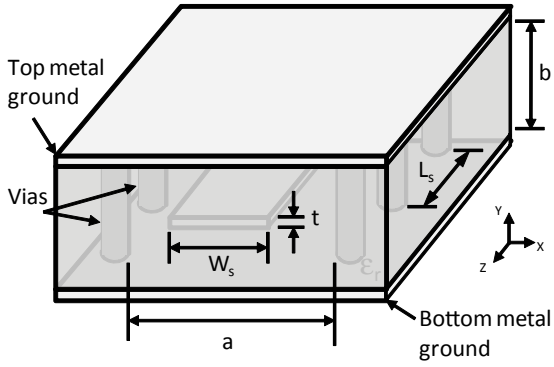

Figure 7.5 Stripline transmission line where W_s is the width of the signal line, t is the thickness of signal line, a is the width between vias, b is the thickness of the dielectric substrate, and L_s is the pitch between vias along the length of the transmission line.

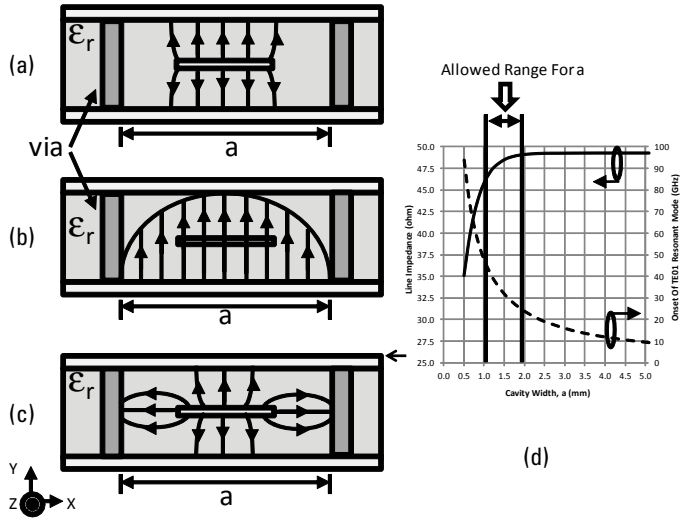

Figure 7.6 Stripline must be chosen carefully so that only (a) the desired mode propagates and (b) not the undesired TE01 mode or (c) the higher loss slot-type mode. (d) The result is that there is a narrow range of allowed values of cavity width (for $\varepsilon_r = 9.8$, b = 1 mm, $w = 0.203$ mm).

$$f_{sr1} = \text{Stripline Cavity Mode} = \frac{v_0}{2a\sqrt{\varepsilon_r \mu_r}} \quad \text{Hz} \tag{7.6}$$

where:

v_0 = speed of light in a vacuum
a = distance between vias (as shown in Figures 7.5 and 7.6)
ε_r = relative dielectric constant = relative permittivity
μ_r = relative permeability.

The other parasitic mode is a type of slot mode in which the strip couples to the vias. The approximate field distribution for it is shown in Figure 7.6(c). This mode is undesirable since it is higher loss than the normal stripline mode due the current distribution on the strip being less uniform and more crowded near the outer edges of the strip. Therefore, an important design parameter for determining the correct distance between vias, *a*, is a balance between avoiding the two parasitic modes. Here is the design challenge: Too large of a distance between vias and the TE_{01} mode will propagate and too small a distance between vias and the slot-type mode will propagate. The difficulty in achieving this is illustrated by the plot in Figure 7.6(d). The plot is the line impedance (solid line) and onset of the TE_{01} mode (dashed line) as a function of cavity width *a*. The line impedance was calculated using the quasistatic variational method.

Appendix B describes the free software tool that was used for the calculation. Note from the plot that a narrow range is allowed for a that is between about 1.1 and 2.0 mm. If a is allowed to increase much larger than 2 mm, then the risk is that the TE_{01} mode will begin to propagate. If a is allowed to be less than 1.1 mm, then the line impedance begins to drop, which means that the strip is coupling to the shorting vias causing the slot-type mode to propagate. This illustrates that not only are the dimensions of the stripline important, but the cavity dimensions must also be chosen carefully.

Another undesired mode in the stripline can exist vertically between the top and bottom ground planes. The frequency at which this mode begins to propagate and create a resonance is determined by the height of the dielectric region given by dimension b in Figure 7.5. The thickness of the substrate should be restricted to less than a quarter of a wavelength thick to avoid higher order mode propagation. The frequency of this resonance is calculated by:

$$f_{sr2} = \text{Stripline Resonant Mode} = \frac{v_0}{4b\sqrt{\varepsilon_r \mu_r}} \quad \text{Hz} \tag{7.7}$$

where b is the thickness of the dielectric (as shown in Figure 7.5).

The design procedure for a buried stripline to avoid resonances and undesired modes is straightforward. Consider the example of a stripline transmission line in HTCC alumina with a dielectric constant of 9.8 and allowed substrate thickness that must be a multiple of 0.125 mm due to available green tape thicknesses with the fabricator. The frequency of operation is 20 GHz. Using these design constraints, design a transmission line that is resonant free as follows:

> *Step 1:* Choose the thickness of the dielectric using (7.7). In most cases, the dielectric material is already determined, which fixes ε_r and μ_r. The maximum operating frequency propagation on the line is also known for most applications, which will determine f_{sr2}. To provide margin, a good design practice is to set f_{sr2} at 10% to 20% higher than is required. We will use a margin of 15% so that our maximum allowed operation frequency, which is the same as $f_{sr2} = 1.15 \times 20$ GHz = 23 GHz. Using (7.7), solve for b, which is the thickness of the dielectric:

$$b < \frac{c}{4f_{sr2}\sqrt{\varepsilon_r \mu_r}} = 1.042 \text{ mm} \tag{7.8}$$

Because the fabricator can only fabricate a dielectric with a thickness that is a multiple of 0.125 mm, we will choose 1.0 mm, which means that the dielectric will be eight layers, each 0.125 mm thick. The signal line will be symmetrically placed in the middle so there will be four layers above and four layers below the signal strip.

Step 2: Next is the determination of the required line width for 50Ω operation. Using a quasistatic variational method of analysis [17], it was found that a line width of 0.203 mm achieves about 50Ω.

Step 3: The final step is to determine the width of the cavity. This is done by choosing the cavity width to be narrow so that the TE_{01} mode does not propagate, and at the same time, choosing the cavity width wide enough that the slot-type mode is not excited on the strip, which will increase the insertion loss. A good trade-off is to keep the change in line impedance to less than 5% and the TE_{01} mode at least 15% above the desired frequency range as illustrated in Figure 7.6(d). For this example, a cavity width of 1.5 mm is chosen. This results in the TE_{01} mode being pushed out to 30 GHz and the change in line impedance is less than about 2%.

Using the design procedure outlined above will result in high-quality stripline transmission line designs for most microwave and millimeter-wave packaging.

7.1.3 Microstrip Lines

Microstrip is possibly the most popular transmission line for use in modules and motherboards. This is due to its ease of use and integration with other circuits. Choosing the materials and transmission line dimensions to achieve 50Ω can be done using most any commercially available transmission line analysis software. Figure 7.7 shows a typical microstrip line and the approximate electric field distribution at the port.

Microstrip structures have three propagating regimes for higher order modes [18]. The first set of modes is in the bound regime with fields that are confined to the metal strip. The fundamental mode is this type of bound mode. The next set of modes is the surface wave mode, which are unguided and propagate away from the axis of the microstrip metal transmission line. The third type of mode is the radiation mode, which radiates from the microstrip into the dielectric and air regions.

The surface wave modes are not desirable because they can be excited by microstrip. The surface wave modes can be TM_n or TE_n modes. These fields decay exponentially in the *X* direction as defined in Figure 7.7. The fields are more confined in the dielectric and near its surface. As frequency increases, the

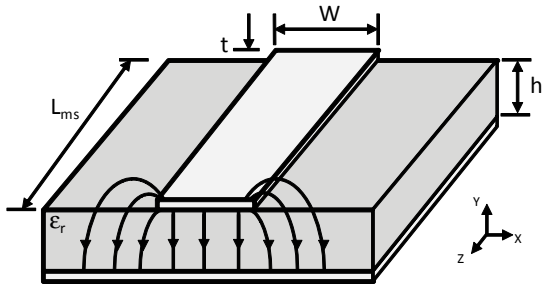

Figure 7.7 Microstrip transmission line showing the approximate port field distribution with metal trace width *W*, thickness *t*, substrate height **h**, and line length L_{ms}.

fields become more tightly bound inside the dielectric. If the dielectric is assumed to extend infinitely in the *Y* and *Z* directions, it is possible to analyze the propagation of the TE_n and TM_n modes and calculate their cutoff frequencies [19] as follows:

$$f_{cTMn} = \frac{nv_0}{2h\sqrt{\varepsilon_r - 1}} \quad \text{for } n = 0,1,2,\ldots \text{Hz} \tag{7.9}$$

$$f_{cTEn} = \frac{(2n-1)v_0}{4h\sqrt{\varepsilon_r - 1}} \quad \text{for } n = 1,2,3,\ldots \text{Hz} \tag{7.10}$$

It is important to note that TM0 has a zero cutoff frequency, which means that it will propagate all the way to zero frequency. It is, therefore, referred to as the dominant slab mode. This means that for any and all dielectric substrates, the TM0 mode is a propagating one.

Another mode that can propagate on a microstrip line is called the transverse higher order mode. It is able to propagate when the width of the microstrip line, *W*, equals a half wavelength. In other words,

$$\frac{\lambda_c}{2} = W \quad \text{meters} \tag{7.11}$$

But we know that $\lambda_c = \dfrac{c}{f_c\sqrt{\varepsilon_r}}$. Therefore,

$$W = \frac{v_0}{2f_c\sqrt{\varepsilon_r}} \quad \text{meters} \tag{7.12}$$

and solving (7.12) for f_c yields

$$f_c = \frac{v_0}{2W\sqrt{\varepsilon_r}} \quad \text{Hz} \tag{7.13}$$

However, this equation does not take into account the fact that the fringing field from the outer edges of the microstrip line results in an effective line width, $W_{ms,eff}$, that is wider than the actual line width, W. Often this is approximated by making $W_{ms,eff} = W + h$, where $W_{ms,eff}$ is the effective width of the microstrip line taking into account the fringing fields.

However, if the transmission line parameters are known, we can calculate the effective line width. The first step in the calculation is recognizing that the capacitance of the microstrip line, neglecting fringing fields, is given by the parallel plate capacitance, noting that the area A is just the line width multiplied by the length of the line, $W \times L_{ms}$, which can be written as

$$C_{pp} = \frac{\varepsilon A}{d} = \frac{\varepsilon W L_{ms}}{h} \quad \text{F} \tag{7.14}$$

The distributed parallel plate capacitance, $C_{L,pp}$, is just C_{pp}/L_{ms}, resulting in

$$C_{L,pp} = \frac{C_{pp}}{L_{ms}} = \frac{\varepsilon W}{h} \quad \text{F/m} \tag{7.15}$$

where:

ε = permittivity = $\varepsilon_o \varepsilon_r$
ε_o = permittivity of free space = 8.854 × 10–12 F/m
W = width of the microstrip line
h = microstrip substrate thickness

and $C_{L,pp}$ is the distributed capacitance of the microstrip line if the fringing fields are neglected. The second step is to recognize that the true line capacitance of the microstrip line can be calculated from

$$Z_o = \sqrt{\frac{L_L}{C_L}} \quad \text{Ohm} \tag{7.16}$$

and

$$v = \frac{1}{\sqrt{L_L C_L}} \quad \text{m/s} \tag{7.17}$$

where:

Z_0 = line impedance
L_L = line inductance of the microstrip line
C_L = line capacitance of the microstrip line
v = velocity of propagation velocity on the line = $v_0 / \sqrt{\varepsilon_{reff}}$
v_0 = speed of light in a vacuum
ε_{reff} = effective dielectric constant of the microstrip line.

Now, by solving for L_L in (7.16) and combining the result with (7.17), we obtain the line capacitance as

$$C_L = \frac{\sqrt{\varepsilon_{reff}}}{Z_0 v_0} \quad \text{F/m} \tag{7.18}$$

Finally, dividing (7.18) by (7.14), equating C_L and $C_{L,PP}$, and solving for W, which is now $W_{ms,eff}$ (the microstrip effective width taking into account the fringing field) results in

$$W_{ms,eff} = \frac{h\sqrt{\varepsilon_{reff}}}{v_0 \varepsilon_o \varepsilon_r Z_0} \quad \text{meters} \tag{7.19}$$

The result is that (7.19) can be used in (7.13) for a more accurate prediction of the transverse resonance mode that will exist on a microstrip line. Combining (7.19) into (7.13) results in

$$f_c = \frac{v_0^2 \varepsilon_o \sqrt{\varepsilon_r} Z_0}{2h\sqrt{\varepsilon_{reff}}} \quad \text{Hz} \tag{7.20}$$

The importance of the width correction can be shown by an example. Consider a transmission line that is 0.5 mm wide on a 0.5-mm-thick substrate with a dielectric constant of 9.8. Using a commercial transmission line simulator, the effective dielectric constant was found to be 6.839 and the line impedance was calculated to be 49.42Ω. Using (7.13), which neglects the fringing field, results in a predicted cutoff frequency of 94.31 GHz, but using (7.20), which correctly accounts for the fringing field, results in a cutoff frequency of 46.37

GHz. Therefore, in this example, (7.13) predicts a cutoff frequency that is twice as high as (7.20).

7.2 Vias for Isolation and Grounding

Vias are used significantly in microwave and millimeter-wave modules and motherboards to achieve grounding of circuits [20]. Typical applications of ground vias are providing isolations between transmission lines and providing ground for passive circuits. At lower frequencies the proper placement of vias for these instances is less critical, but for microwave and millimeter-wave packaging, proper placement of vias is critical. In this section, we consider two cases for proper via grounding: a ground pad that may be used as a QFN or MMIC ground pad and isolation between stripline transmission lines.

Consider a pad as shown in Figure 7.8(a), which is typically used as a ground pad for an MMIC or for a QFN package. It has an array of vias to connect the metal pad to the ground plane below the dielectric. The vias must provide sufficient ground contact. At DC or low-frequency applications, a single via may be sufficient. However, at microwave and millimeter-wave frequencies, the ground pad will support parasitic resonances and will conduct signals across the pad. Therefore, vias must be carefully placed [21]. Because of the periodic structure of the via array, it can be considered a photonic bandgap structure [22]. The result is that above a certain frequency the ground pad performs as a filter rather than an rf ground, and it exhibits parasitic coupling and resonances. Therefore, the via diameter and pitch must be chosen so that the resonances are pushed beyond the operating frequency.

The via fence structure can be modeled using a lumped element equivalent circuit shown in Figure 7.7(b). The ground pad metal between each via fence can be modeled as parallel plate line impedance given by

$$Z_l = \sqrt{\frac{\mu_0}{\varepsilon_0 \varepsilon_r}} \frac{h_S}{d_{lat}} \quad \text{ohm} \tag{7.21}$$

where hS is the height of the substrate (from the pad to the lower ground) and d_{lat} is the pitch between the via fences in the Z direction as shown in Figure 7.8(a).

The series inductance, L_1, in the equivalent circuit represents the current flow in the Z direction as defined in Figure 7.8(a) and a portion of the via inductance. The shunt inductor, L, is related to the via mutual inductance and C is defined by the first resonance in the Z direction. The values of the equivalent circuit are determined by extraction from electromagnetic simulations.

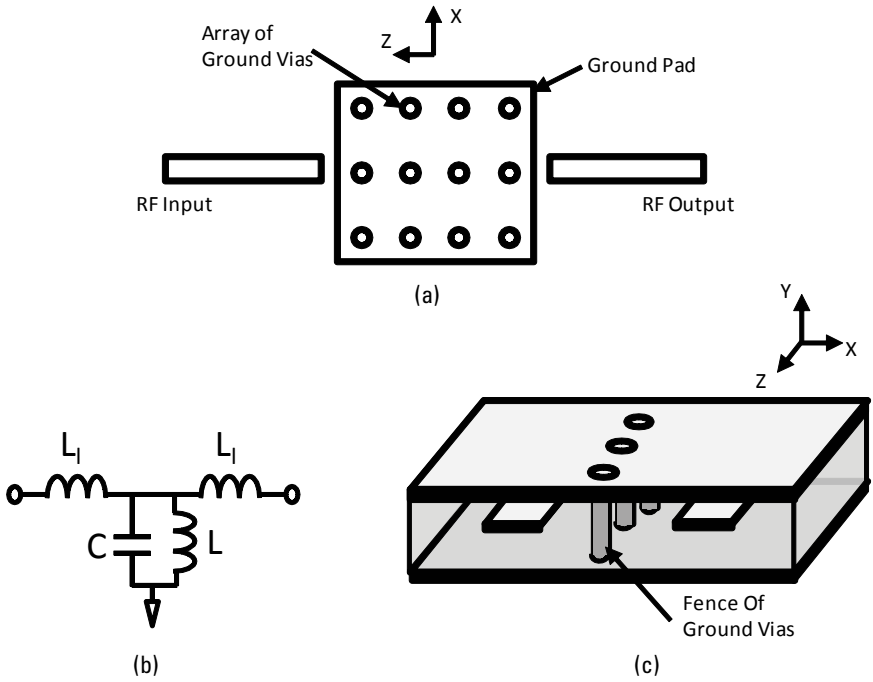

Figure 7.8 (a) Vias are used to ground metal pads used for MMIC and/or QFN mounting. (b) The via fence can be modeled as an LC network. (c) Vias are also used to isolate transmission lines.

In practice, full 3D electromagnetic simulations are conducted to determine the resonances and determine the proper placement of the vias.

Grounding vias are also used to isolate transmission lines. For instance, it is very common for isolation vias to be used to isolate CBCPW transmission lines or to isolate stripline transmission lines. Figure 7.8(c) shows how a fence of ground vias can be used to isolate two stripline transmission lines [23, 24].

7.3 Cavity Resonances

In Section 1.1.2, package resonances were discussed. Package resonances are created in modules if a metal housing is used and in motherboards when a metal shield is used. In both cases, the metal creates a resonant cavity mode, which will couple to the transmission lines and create high insertion loss at the resonant frequency. In most cases, these resonances will inhibit or completely restrict proper operation of the circuits in the module or motherboard at the frequency of resonance. This resonance was traditionally referred to as the "lid effect" when a metal lid is placed on top of a metal housing because the reso-

nances would appear on the network analyzer when the module is tested [25]. In Section 1.1.2, the resonance was accurately modeled as longitudinal section magnetic (LSM) modes. It was also found that the lowest cutoff mode in a dielectric filled cavity is the LSM11 mode and a very accurate method of predicting that mode was presented.

One method for avoiding the cavity mode is to simply choose the dimensions of the package in the case of a module or the shield in the case of a motherboard so that the first resonant mode is pushed beyond the highest operating frequency.

In a more general treatment of cavity modes and their suppression [26], the cavity can be analyzed as a 3D resonator that can support modes in all three directions (*X, Y, Z*) as defined in Figure 1.3. The resonance creates high-*Q* insertion loss poles. The effects of the resonance(s) can be minimized by reducing their *Q*. One way of doing this is to place a damping dielectric substrate with a resistive film on the inside of the package lid [27]. Damping of the cavity mode was found to be most effective when the damping substrate has a higher dielectric constant. This is due to the fact that the tangential electric field at the interface between the substrate and air increases with increasing substrate dielectric constant. The tangential electric field is responsible for the surface currents in the resistive film. Optimum values for resistive film are between 10 and 20 Ω/square with a thickness of 100 to 1,000 Å. This technique is an alternative to using absorber material.

The more traditional method is to use an absorber material. These materials have very high values of permittivity and permeability. In addition, they have very high loss. As a result, when they are added to the lid of a module or a shield, they absorb the electromagnetic fields and convert the energy into heat, which is dissipated. The result is that the quality factor of the resonance is reduced so that less energy, from the circuits on the module or on the motherboard, is coupled into the cavity mode. Absorbers are fabricated from polymers, silicon, or urethane loaded with iron and ferrites. In addition to reducing the effects of cavity resonances, absorbers on the lid will reduce coupling between circuits [28].

Questions

1. What is a zero cutoff mode?
2. How can the undesired propagating modes in CBCPW be suppressed?
3. What pitch between vias should be used to ensure resonance-free operation of a CBCPW line to 50 GHz?

4. What is the frequency for a stripline cavity mode for a cavity width of 2 mm, cavity thickness of 1 mm, and an LTCC ceramic with a dielectric constant of 7.8?
5. What is the maximum thickness for a stripline substrate to ensure the stripline resonant mode between the top and bottom grounds does not propagate for an LTCC module with a dielectric constant of 7.8 operating at 25 GHz?
6. What two limits determine the range for a proper stripline cavity width? How is each calculated?
7. What are the first three TE and TM surface wave modes for a microstrip line with a dielectric constant of 9.8 and a thickness of 0.75 mm? Tabulate them and comment on the bandwidth over which a substrate of this thickness might be useful for microstrip lines.
8. What is the frequency of the first transverse resonance in for a 50Ω microstrip line on 0.75-mm-thick alumina ($\varepsilon_r = 9.8$)?

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8

Transitions and 3D Packaging

A transition is a connection that exists between dissimilar signal transport structures. At microwave and millimeter-wave frequencies, the characteristics of transitions are very different than for low-frequency applications. Often, one or both of the signal transport structures is a transmission line that must be properly designed at high frequencies but is not a concern at DC or low frequencies. An example of a transition between two transmission lines is the connection between a microstrip line and a coplanar waveguide. Another unique feature of high-frequency transitions is that they rarely occur at a single point; instead, they can include an intervening circuit consisting of metal and dielectric features. The goal in most cases is to minimize the size of the transition structure, but in other cases an electrically large transition structure is required to include matching circuitry or field transitions. Undesired parasitics and higher order modes at these transitions are also a challenge. Three-dimensional packaging, in which substrates or integrated circuits are stacked on top of each other, make extensive use of transitions, especially vertically. These and other characteristics make transition design at microwave and millimeter-wave frequencies more challenging than at lower frequencies.

The first type of transition to be discussed in this chapter is between transmission lines. Transitions can be on the same surface as with a microstrip to CBCPW transition or between a surface transmission line such as microstrip and a buried transmission line such as stripline. The chapter concludes with an examination of 3D packaging at both the substrate and IC levels. The emphasis of this chapter is on developing equivalent circuits for transitions and on introducing a few important transition types.

8.1 Transitions Between Transmission Lines

This section discusses the general design approach to ensure wideband transitions between different transmission line types with practical design examples of a transition between CBCPW and microstrip and between microstrip and stripline in a multilayer package.

Transitions between transmission lines have the widest bandwidth possible when some general guidelines are followed:

1. *Maintain the same field distribution between transmission lines.* This is difficult to achieve in practice because dissimilar transmission lines have dissimilar field distributions. In practice, the transition structure can often be modified to improve the transition of the fields. Very wide band transitions are possible if the field distributions are maintained.
2. *Smoothly transition between transmission line types.* Rather than using abrupt transitions between signal transport structures, it is beneficial to smoothly transition the metal or dielectric structure of one transmission line into another. The reason is that abrupt changes in the metal or dielectric structures often generate higher order modes. Even though the higher order modes are evanescent (i.e., cannot propagate), they can result in stored energy at the transition point. This stored energy will appear as undesired series inductance or shunt capacitance. This is especially true for multilayer boards and modules.
3. *Use impedance transformation when appropriate.* At times, a transition from one transmission line to another will actually require the use of an intermediary transmission line to achieve an impedance transformation. In these cases, use the intermediary transmission line to impedance match the transition and transition the fields. For instance, a section of quasi-coax (formed using vertical vias) cannot be designed to support the system impedance, which will require the creative use of impedance transformation at the transition. Alternatively, the physical features of the quasi-coax can be optimized to aid in the impedance transformation.
4. *Minimize stray capacitance.* The bandwidth of transitions is often limited by stray capacitance that exists between the signal conductor and the surrounding grounding structure. It can be created by capacitance at via catch pads, isolation vias, vertical transitions, and at transitions to connectors.
5. *Avoid the excitation of propagating higher order modes.* This is normally accomplished by proper transmission line design to support only a single propagation mode. However, some convenient connectors and

transition structures can support multiple zero cutoff modes. In these cases, it is important to use the metal and dielectric features of the transition to suppress or avoid the excitation of the undesired modes.

8.1.1 CBCPW to Microstrip Transition

Transitions between coplanar waveguide and microstrip are used frequently. For instance, they are used in MMIC chips as the probe pad to microstrip transition. Also, CBCPW to microstrip transitions are used in motherboards and modules to make connections between transmission lines to accommodate circuit requirements. For instance, some surface-mount QFN-style plastic packages require the use of a ground–signal–ground connect for which CBCPW is used, but the rest of the module may need to use microstrip for other circuits. In these instances, a transition is used between the CBCPW line and microstrip.

The design of this transition can be achieved by using an abrupt connection as shown in Figure 8.1(a). Note how the CBCPW section has a double row of vias. If only a single row is used next to the signal line, coupling will occur along the outside edge of the CBCPW ground. This coupling will result in parasitic resonances.

Often, the ground of the CBCPW is tapered in the region of the transition to the microstrip as shown in Figure 8.1(b). A tapered transition is used to achieve a gradual transition of the ground plane to the CBCPW mode. The taper is formed by gradually decreasing the line width and gap to the outside ground and maintaining constant 50Ω impedance at each step in the transition.

The abrupt transition was simulated in HFSS and the results are shown in Figure 8.1(c). The figure shows that even an abrupt transition achieves acceptable performance in the millimeter-wave range.

8.1.2 Cofired Ceramic Microstrip and Stripline Transition

A commonly used transition in multilayer circuit boards is the transition between microstrip and a buried stripline as shown in Figure 8.2(a). This type of transition allows for the rf signal to be routed in buried layers under ICs and other components that are mounted on the top surface. The buried ground, GND1, provides ground reference for the microstrip line as well as the top ground reference for the stripline. GND1 has an opening, d, for the signal via from the microstrip line. The lower ground, GND2, provides the lower ground reference for the stripline circuit. The microstrip line is connected to a single via that transitions the rf signal 90 degrees to the lower microstrip line.

Some applications may have multiple ground layers at GND1. For those situations, surrounding this signal via is a ring of ground vias that approximates

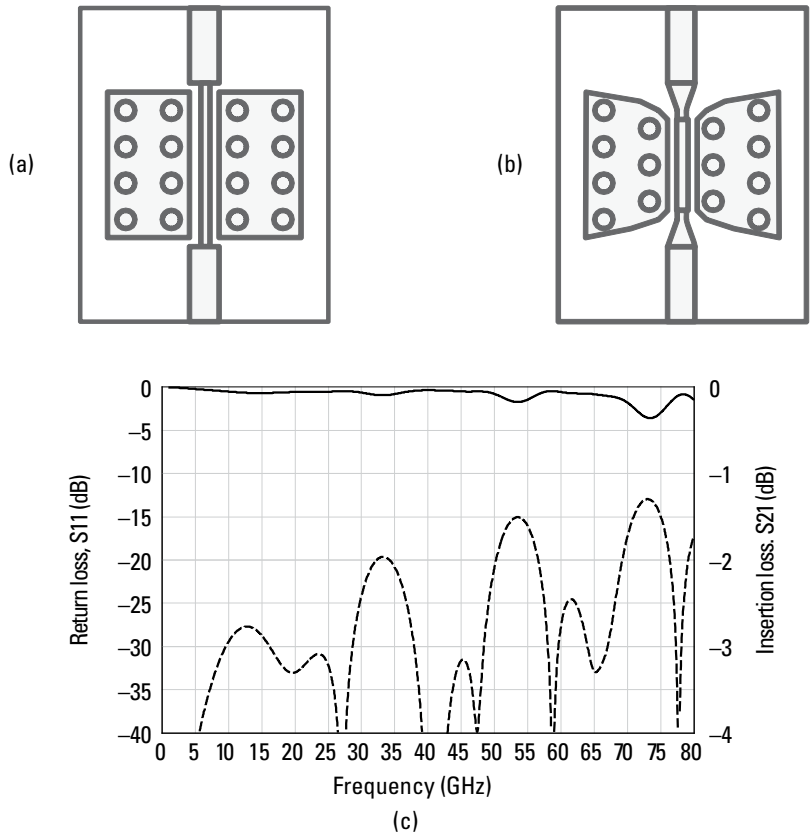

Figure 8.1 The transition between microstrip and CBCPW can be achieved using (a) an abrupt (i.e., no taper to the CBCPW ground plane) transition or (b) a smooth transition. (c) The optimized simulated performance of the abrupt transition functions to 80 GHz as shown by 3D electromagnetic (EM) simulations in HFSS.

the outer ground structure of a coaxial transmission line. Several important design parameters must be considered when using this type of transition:

1. The opening, *d*, in the top ground, GND1, affects the performance of the transition. It can be used as a tuning element. Narrowing this opening causes a shunt capacitive effect on the signal via. Widening the opening causes an inductive effect on the microstrip line since a larger opening removes the ground from underneath the microstrip line.
2. The number of vias surrounding the signal via impacts the impedance of the via section and isolation to surrounding circuits. Increasing the number of vias improves isolation by reducing the amount of signal that can radiate in the lower levels of the circuit. This is important

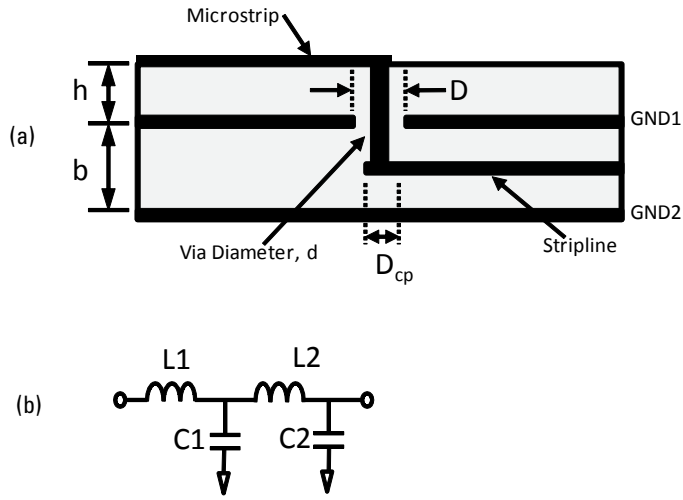

Figure 8.2 A microstrip to stripline transition is frequently used in multilayer ceramic modules and laminate motherboards. (a) A simplified version uses only a single via connecting the microstrip and stripline. (b) A simplified equivalent circuit of the signal transition can be used.

because radiation to surrounding circuits can create oscillations and undesired resonances.

3. The distance from the signal via to the surrounding vertical ground vias should initially be chosen to approximate a 50Ω coaxial transmission line. Then, using 3D EM simulations, the distance from the signal via to the surrounding vias can be optimized for electrical performance.
4. Parasitic capacitance at the signal via to stripline connection can limit the electrical bandwidth of the transition. The stray capacitance is caused by the via catch pad on the stripline signal trace at the point where it contacts the vertical signal via. This catch pad, which is normally required by the package manufacturer, is typically wider than the stripline transmission line, which results in undesired shunt capacitance. Another source of stray capacitance is the signal via itself coupling to the lower ground plane. One method to address this issue is to lower the ground plane in the vicinity of the via to stripline connection point [1].

An equivalent circuit of the via interconnect can take on several different forms [1, 2]. Figure 8.2(b) shows a simplified equivalent circuit using lumped inductors and capacitors.

The via inductance, L1 and L2 of the model, can be approximated by the inductance of a via in microstrip given by [3]

$$L_{via} = \frac{\mu_0}{2\pi}\left[h \cdot \ln\left(\frac{h + \sqrt{r^2 + h^2}}{r} \right) + \frac{3}{2}\left(r - \sqrt{r^2 + h^2} \right) \right] \quad \text{H} \tag{8.1}$$

where h is the length of the via (i.e., the thickness of the substrate) and r is the radius of the via.

Note that the units for the variables used in (8.1) must be in meters. Capacitance C_1 of the equivalent circuit is mainly due to via coupling to the opening in the ground plane. The capacitance of that section can be approximated by considering that section to be a very short section coaxial transmission line. The length of the coaxial section is just the thickness of the ground plane, which is short indeed. The capacitance of a section of coaxial line can be determined by first finding the line capacitance as

$$C_{\text{line capacitance}} = \frac{1}{v_o Z_o} \quad \text{F/m} \tag{8.2}$$

For coaxial line,

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(D/d \right) \quad \text{ohm} \tag{8.3}$$

Substituting (8.3) into (8.2), it is easy to obtain

$$C_{\text{coax line capacitance}} = \frac{\varepsilon_r}{60 \cdot v_o \ln\left(D/d \right)} \quad \text{F/m} \tag{8.4}$$

where:

ε_r = effective dielectric constant of the substrate material
D = the ground plane opening
d = diameter of the via.

However, the ground plane opening creates a fringing field to the via that makes the coaxial section appear to be electrical longer. The physical distance of the fringe field can be approximated and a scaling factor that is structure dependent can be used. With these approximations, the capacitance is give by

$$C_1 = A_1 \cdot \left(h + \frac{b}{2} \right) \frac{\varepsilon_r}{60 \cdot v_o \ln\left(D/d \right)} \quad \text{F} \tag{8.5}$$

Capacitance C_2 is mainly due to stray capacitance from the stripline to via connection. This structure is formed by a catch pad that is connected to the stripline and the via. The resulting capacitance can be estimated by considering it to be a parallel plate capacitor of area equal to the area of the stripline via catch pad, which has diameter of D_{cp} and is separated from the ground plane by $b/2$. Therefore, the area is given by

$$\text{Area of stripline catch pad} = A_{cp} = \pi\left(\frac{D_{cp}}{2}\right)^2 \quad m^2 \tag{8.6}$$

$$C_2 = \frac{A_{cp} \cdot \varepsilon_o \varepsilon_r}{\text{spacing}} = \frac{\pi\left(\frac{D_{CP}}{2}\right)^2 \varepsilon_0 \varepsilon_r}{b/2} \quad \text{F} \tag{8.7}$$

where:

A_{cp} = area of the stripline catch pad
D_{cp} = diameter of the stripline via catch pad
b = thickness of the stripline dielectric
ε_r = dielectric constant of the substrate
A_1 = constant that depends on the geometry and materials and is equal to ~0.5.

The capacitance that is predicted by (8.7) is lower than the actual capacitance created by the stripline catch pad. This is due to the fringing field that exists at the stripline catch pad. This capacitance can be a concern and can limit the bandwidth of the transition. Significant effort is often expended to reduce this capacitance [1]. An improved model for C_2 is to estimate that the fringing field increases the effective radius of the stripline catch pad by half the thickness of the dielectric between it and the lower ground plane. With this improvement to the capacitance approximation, the effective area of the stripline catch pad becomes

$$A'_{cp} = \pi\left(\frac{D_{cp}}{2} + \frac{b}{4}\right)^2 \tag{8.8}$$

This increases the area of the catch pad, which increases the value of C2 so that (8.7) now becomes

$$C_2' = \frac{A_{cp}' \cdot \varepsilon_o \varepsilon_r}{spacing} = \frac{\pi\left(\frac{D_{CP}}{2} + \frac{b}{4}\right)^2 \varepsilon_0 \varepsilon_r}{b/2} \tag{8.9}$$

A microstrip to stripline transition was modeled in HFSS. The equivalent circuit was developed using the schematic from Figure 8.2(b) and using (8.1), (8.5), and (8.9) to calculate the parameter values. The results are shown in Figure 8.3, which compares the HFSS model simulation to the simulation from the equivalent circuit.

Though the equivalent circuit developed for this transition shows good agreement, a higher fidelity model than the one from Figure 8.2(b) can be developed. For instance, the section of microstrip that makes contact with the via has a higher impedance. This is due to the fact that the ground plane underneath it is removed since it forms the opening for the via to extend down to the stripline. Including the increased line impedance can improve model fidelity. The contact point of the via and the microstrip line can experie nce stray capacitance if a large catch pad is required over the via. For some processes, larger catch pads are required for topside vias than for buried vias. Including a capacitance in the model for this effect can improve the fidelity of the model. The stripline section that contacts the via also has a higher impedance due to the opening in the ground plane. An improved model should account for these and other effects in the transition.

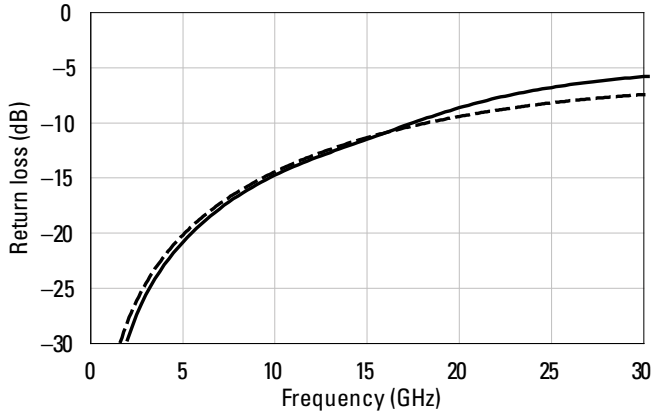

Figure 8.3 Comparison of the HFSS and equivalent circuit for the microstrip to stripline using LTCC with $\varepsilon_r = 7.8$, $h = 0.25$ mm, $b = 0.5$ mm, $D = 0.55$ mm, $d = 0.2$ mm, and $D_{cp} = 0.35$ mm, which yields equivalent circuit values of L1 = 0.0259 nH, L2 = 0.108 nH, C1 = 0.102 pF, and C2′ = 0.0781 pF.

The transition from microstrip to stripline considered in this section uses a single connecting via between the microstrip and stripline. Often, however, there are multiple layers between the microstrip and stripline. In these instances, multiple vias must be used to properly transfer both the signal and the ground currents. One method is to use three-wire line to perform the transition [4, 5]. In this configuration, the signals and ground are transitioned using a three-wire transmission line. One drawback of this method is that it does not achieve the isolation that other methods are able to achieve and it is prone to the excitation of undesired modes. A preferred method is to use multiple vias [1] or to form a quasicoaxial vertical transmission line.

8.1.3 Laminate Board Microstrip to Stripline Transition

The transition from a surface transmission line to a buried transmission line in a laminate circuit board can be more difficult than for a cofired ceramic board. This is due to the fact that laminate circuit boards often have the design constraint that blind vias cannot be used because of their increased cost. Processing blind and buried vias in laminate boards increases costs because additional manufacturing processing steps are required. The aversion to additional cost is a strong motivator for laminate circuit board design choices. Therefore, blind vias are often not used and the transition design must proceed with only through-hole vias. This is rarely a concern for low-frequency or DC packaging, but can be a concern and can create performance issues for microwave and millimeter-wave motherboards. This can be a design concern because the through-hole via extend beyond the connection point to the stripline transmission line. The result is a stub of metal that can add parasitic capacitance, generate undesired signal radiation, and resonate at high frequencies [6, 7]. This can be of particular concern for board designs that have multiple layers below the stripline transmission line because it will result in a longer stub. Figure 8.4 illustrates this case and shows the via stub extending beyond the end of the stripline section.

One solution for this is to back-drill the via extension. If this process is used, then the stub created by the via extending beyond the stripline is drilled so that the metal is removed. This process works, but adds cost to the fabrication process. It also introduces variability in the transition performance since it is difficult, in practice, to hold tight tolerances on the depth of the drill as it removes the via stub. This solution is effective in removing the majority of the stub, although a small stub remains because the drill depth is never equal to the full stub length.

$$C_3 = A2 \cdot \frac{b}{2} \frac{\varepsilon_r}{60 \cdot v_o \ln\left(D/d\right)} \tag{8.10}$$

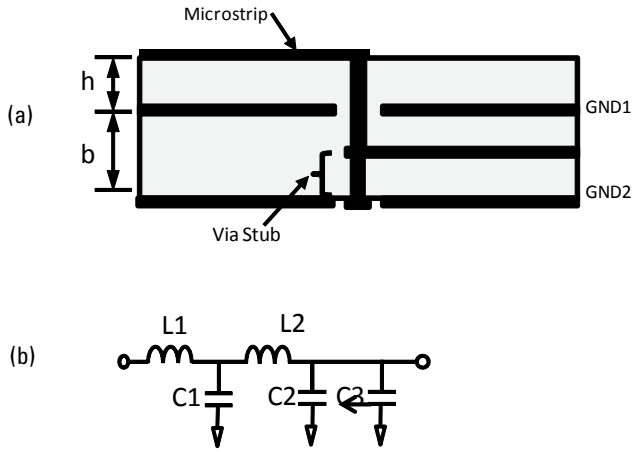

Figure 8.4 A laminate transition from microstrip to stripline will have a via stub extending beyond the stripline contact if only through-hole vias are used for low-cost laminate boards.

where the $A2$ constant depends on the geometry and materials and is equal to ~0.75.

8.2 Three-Dimensional Packaging

Three-dimensional packaging involves the stacking of substrates or integrated circuits with interconnects between layers. An example of an interconnect between stacked substrates is a compressible three-wire line, which has been used between stacked substrates in modules for phased-array radar [8, 9]. Other transitions between stacked integrated circuits use wire bonds to connect one layer to the next.

8.2.1 Stacked Substrate Solderless Interconnects

A practical example of a 3D module formed by stacked substrates is shown in Figure 8.5(a). It is a 3D structure with four transmit/receive (T/R) modules. Its volume is approximately 30.5 mm × 30.5 mm × 10.2 mm. The T/R functions are achieved using GaAs MMIC flip chips, Si IC flip chips, and miscellaneous passive components. Figure 8.5(a) shows three ceramic substrates stacked on top of each other and separated by ring frames. In general, this method can accommodate two or more stacked substrates or layers. The ring frames serve as a physical spacer between substrates, provide a heat transfer path between substrates, and capture the solderless interconnects that exist between the substrates. This type of module and variations of it have been produced in high volumes for several different applications.

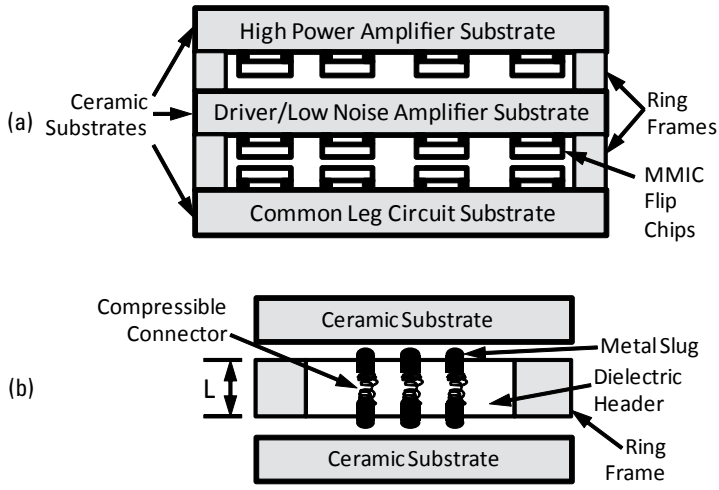

Figure 8.5 (a) The tile array module uses stacked substrates that are separated by ring frames. (b) Solderless interconnects exist in the ring frame and are contained with dielectric headers. (© 1997 IEEE. From [9]. Reprinted with permission.)

The solderless interconnects can be formed many different ways [10, 11] and can directly contact the surface of the substrates, or a metal slug can be used at either end of the compressible element to contact the substrates. The compressible section serves as a spring to allow for solderless connections and as a path for the rf signal to pass. This is illustrated in Figure 8.5(b), which shows how two ceramic substrates are compressed together with a three-wire compressible interconnect. The three wires form a type of transmission line. The three parallel conductors are imbedded in a dielectric material.

A close-up image of a compressible connector is shown in Figure 8.6. It shows the compressible connectors without their dielectric header, which is used to mechanically capture and protect it. This type of compressible connector is created by randomly forming a 0.0254-mm wire into a cylindrical shape. It results in an electrical connection that can support both DC and high-frequency signal propagation.

The goal is for the compressible interconnect to have its line impedance matched to the transmission lines that are on the substrates. Figure 8.7(a) shows the cross section of a three-wire line and the dimensions of the dielectric header. In this configuration, the dielectric header is enclosed in metal, which is the ring frame separating the substrates. The dimension x of the dielectric header is selected to avoid the first waveguide mode, which is given by

$$f_c = \frac{1}{2a\sqrt{\varepsilon_r}} \tag{8.11}$$

Figure 8.6 Compressible connectors with a diameter of about 0.5 mm. (Courtesy of Custom Interconnects, LLC., Centennial, CO.)

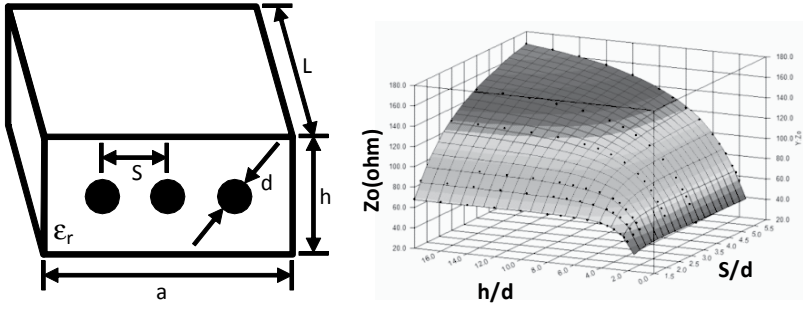

Figure 8.7 The compressible interconnect can form (a) three-wire transmission lines and (b) can be designed for 50Ω impedance by selecting the correct shape ratio (S/d) depending on the dielectric constant of the header that captures the compressible connector. (Curve-fit equation courtesy of Curvefitting.com.)

where a is the width of the dielectric header in the metal ring frame and ε_r is the dielectric constant of the dielectric header material. The minimum dimension for the width of the dielectric header, *a*, is the practical limit on the minimum amount of dielectric material that can remain on either side of the three-wire line formed by the compressible connector.

The height *h*, diameter *d*, and spacing *S* between the compressible connectors were determined by performing a set of HFSS simulations. The 3D plot is shown in Figure 8.7(b) and gives the line impedance as a function of

the shape ratios *S/d* and *h/d*. The impedance is given for a dielectric of air. For dielectric constants greater than unity, divide the impedance by the square root of the dielectric constant. The impedance of the three-wire compressible connector is given by the following curve-fit equation:

$$Z_o = \frac{1}{0.00454 + \frac{0.001018}{S/d} + \frac{0.01708}{h/d} + \frac{0.02154}{(S/d)^2} + \frac{0.02963}{(h/d)^2} + \frac{-0.03287}{\left(\frac{S}{d} \cdot \frac{h}{d}\right)}} \tag{8.12}$$

Multiple parasitic effects must be considered when using compressible connectors at microwave and millimeter-wave frequencies. One of the effects is the previously mentioned waveguide mode, which can exist within the dielectric header. Because the compressible connector has four conductors (three compressible contacts and the outside ground), it can support three zero cutoff modes. It is important to properly design the compressible connectors to avoid the excitation of those modes.

Another parasitic effect is a resonance that can be excited along the length of the compressible connector. Because this effect occurs along the length of the transmission line, it can be referred to as a transmission line resonance. This is often the dominant effect that limits the length *L* or the maximum frequency at which the compressible connector can be used. This resonance exists along the length of the connector, *L*. If the compressible connector is symmetrically terminated, then the excitation of this mode can be pushed to a half wave resonance.

Figure 8.8 shows a simplified schematic of the three-wire line compressible interconnect transition between the motherboards. It shows the transmission line that exists on each of the motherboards and the transition impedance, Z_T, that exists at the point at which the signal transitions from the motherboard into the three-wire line. If that terminating impedance is symmetrical such that $Z_{T1} = Z_{T2}$, then the resonance that exists along the three-wire line will appear

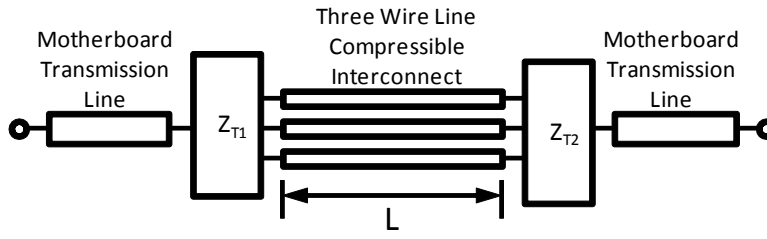

Figure 8.8 The transition point between the motherboards and the compressible vertical interconnect causes an impedance, Z_T.

at a half wavelength. If, however, the terminating impedance is not symmetrical such that $Z_{T1} \neq Z_{T2}$, then the undesired resonance will occur at a quarter wavelength. The resonant frequency of the quarter wave and half wave resonance are given by

$$f_{r,\lambda/4} = \frac{v_o}{4L\sqrt{\varepsilon_r}} \tag{8.13}$$

$$f_{r,\lambda/2} = \frac{v_o}{2L\sqrt{\varepsilon_r}} \tag{8.14}$$

The dielectric header is often terminated at the motherboard connection point in a significant amount of ground metal. This can cause the dielectric header to perform as a waveguide resonator. The waveguide resonance mode is predominantly determined by the length L of the dielectric header inside the metallic ring frame. The resonance frequency for this mode can be approximated by the familiar rectangular waveguide resonator equation [12]:

$$f_r = \frac{v_o}{\sqrt{\varepsilon_r}}\sqrt{\left(\frac{m}{2a}\right)^2 + \left(\frac{n}{2h}\right)^2 + \left(\frac{p}{2L}\right)^2} \tag{8.15}$$

where:

v_0 = speed of light in a vacuum
a = width of the dielectric header
h = height of the dielectric header
L = length of the dielectric header
m, n, p = waveguide mode indices
ε_r = dielectric constant of the dielectric header.

The primary cavity resonance mode is the TE_{101} mode ($m = 1$, $n = 0$, $p = 1$) with the assumption that the width of the header is greater than the height, which will be the case for the vast majority of practical applications. Practically speaking, the resonant frequency of this mode is less of a concern since it is normally well above the frequency of transmission line resonance mode.

Variations of the compressible connector include a coaxial version, which uses a compressible center conductor and outside ground formed by solid metal, vias, or other compressible connectors. A differential signal version of the

compressible connector is possible that uses two compressible contacts and a ground reference.

8.2.2 Highly Integrated Modules with Vertical Transitions

By considering the package as part of the overall circuit rather than as a separate component, package design can be approached as an integral part of product development. This can result in significant cost, size, and weight savings. Consider the system-in-package example of a 10-GHz module, which can be used for either communications or a radar system [13]. Figure 8.9(a) shows a simplified block diagram of the system. The completed module includes a radiating antenna, MMIC amplifiers, a mixer, rf switches, bias capacitors, wire bonds, and a package that can be integrated onto an FR-4 or other laminate substrate.

In this example the vertical transitions make contact with the motherboard using solder balls as shown in Figure 8.9(b). The package is a mixed material solution that uses a low-permittivity antenna to achieve good radiation efficiency. The rest of the package uses a good-quality microwave laminate. The package is mounted with the antenna facing away from the motherboard.

A few concerns are associated with this package, for example, the stress that is induced from the CTE mismatch that can exist between the package and motherboard. Any such stress will work the package lamination points and may become a source of failure. Another concern is unwanted radiation, which is

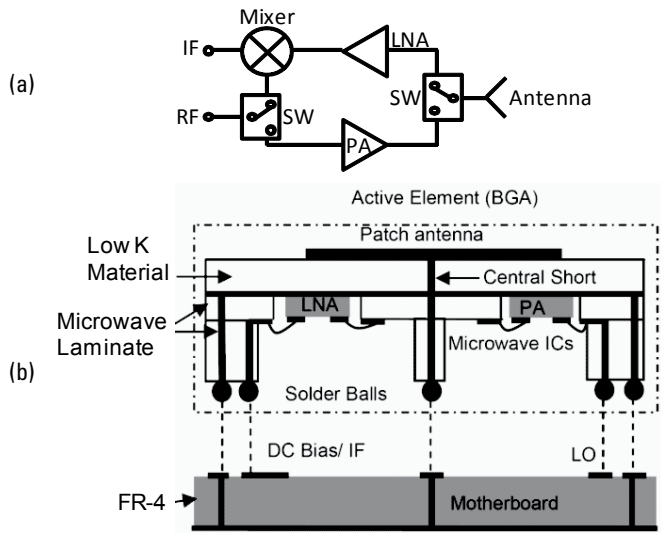

Figure 8.9 Using a highly integrated system-in-package approach it is possible to (a) integrate a transceiver into (b) a package that includes the antenna and all components. (© 2005 IEEE. From: [13]. Reprinted with permission.)

caused by the vertical via transitions, from this package to surrounding circuits. The vertical via transitions will also radiate into the package, which may be a source for feedback oscillations. The gain of the module should be investigated carefully to avoid these concerns. However, this packaging approach can be a low-cost solution especially if combined with low-cost, integrated circuit processing such as SiGe or other low-cost processes.

8.2.3 Using the Package as a Circuit Element: An Integrated 60-GHz Module

Significant innovation can be achieved at millimeter-wave frequencies by using the package as part of the module. An example of this is using the package lid as part of the antenna system, as was achieved at 60 GHz. Figure 8.10 shows a 60-GHz package that contains a transceiver integrated circuit and an antenna substrate. On transmit, the signal from the IC is carried to the antennas, which radiate the signal. Because of the high frequency being used, the lid has a significant effect on the millimeter-wave signal propagation through it. Therefore, the lid must be properly designed to pass the 60-GHz signal. The antenna energy can be focused by integrating a dielectric lens into the lid of the package. The lens will improve the gain of the antenna, thereby improving system-level performance [14].

8.2.4 Three-Dimensional Integration by Stacking ICs and Packages

Various 3D packaging technologies are being used. Some of the technology choices include [15]:

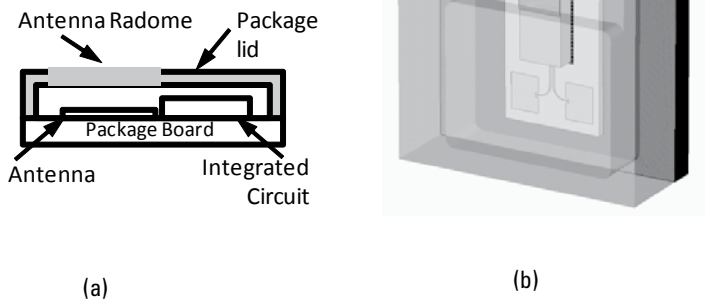

Figure 8.10 Example of a system-in-package approach to the design of a 60-GHz transceiver system. (Courtesy of VubIQ, Irvine, CA.)

- Die on die using wire bond interconnects;
- Die on die using through-silicon-vias;
- Die on wafer;
- Wafer on wafer;
- Stacked die + stacked wafer;
- Package on package.

Other technologies are being used or proposed for use that extend the methods mentioned above. However, the 3D packaging has its design challenges. For example, thermal management is a significant concern for microwave and millimeter-wave applications where the heat densities of high-power devices can be as high as 1,000 W/cm^2 or even higher. For applications that dissipate lower power levels, the heat transfer challenges are easier to manage. The thermal issue in 3D packaging is that as the package stack grows, the heat generated by the uppermost die or package must be transferred through the lower levels. Innovations in thermal management materials may help address these challenges. Proper material choices, parts placement, and layer planning are other ways to address this challenge.

Test and measurement can be a challenge. Although the 3D packaging assumes that known good dies are used at the start of the integration process, the testing becomes more complicated. This is partly due to the fact that some circuits are so highly embedded in the 3D system that direct access is not possible. This can be especially challenging for circuits that must be programmed prior to shipment. Therefore, careful design for testability is critical for success.

The cost and complexity of a 3D system adds to the risk of development and production. At the end of the integration process, the value added to the product is significantly higher than for each of the individual components. Therefore, the cost of scrap product is much more significant. Furthermore, the installed base of manufacturers that can handle these complex processes, though growing, remains small. Therefore, the cost of manufacturing remains high except for those with the capital required to create the required processes.

Regardless of the challenges, highly integrated 3D systems at microwave and millimeter-wave frequencies are being developed and will become another option for the product developer.

8.3 Conclusions

Transitions form a critical part of most microwave systems. They allow for signals to be transported between locations and between circuits. This chapter focused on the general concepts involved in transition design and provided a

few examples. The chapter concluded with a discussion on 3D packaging and the design of systems-in-package solutions for microwave and millimeter-wave solutions.

Questions

1. Calculate the inductance of 0.1-, 0.2-, 0.3-, 0.4-, and 0.5-mm-diameter vias that connect through a substrate that is 1.5 mm thick. Generate a curve of inductance versus via diameter.
2. Using the transition dimensions give in the caption of Figure 8.3, calculate the increase in capacitance using (8.9) versus using (8.7). What effect does this capacitance have on the bandwidth of the package?
3. Calculate the model parameters for a microstrip to stripline transition using the same dimensions as shown in the caption of Figure 8.3 except for a substrate dielectric constant of 2.2 (low K laminate) and 9.2 (HTCC alumina ceramic). Use the two models to compare the electrical bandwidth of the two transitions.
4. Using the dimensions given in the caption of Figure 8.3, determine the opening in the ground plane, D, required to lower its capacitance to be less than the capacitance caused by the stripline catch pad. Be sure to use the improved formula for the stripline catch pad capacitance.
5. Calculate the TE_{101} cavity resonance mode for a three-wire compressible connector as shown in Figure 8.7 with cavity dimensions of $a = 2$ mm, $h = 1.5$ mm, and $L = 5$ mm with a relative dielectric constant of 2.2.
6. Calculate the quarter wave and half wavelength resonances in a compressible connector (shown in Figure 8.7) using the same cavity dimensions given in Question 5. What is the maximum safe operating frequency of this compressible connector assuming the quarter wave resonance is not excited?

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9

Heat Transfer

As demonstrated in Chapter 1, thermal effects in microwave and millimeter-wave electronic packaging can be much more significant than for lower frequency electronics. This is due to the fact that the heat flux (or heat density) is large, especially for high-power amplifiers. The increased heat flux has a direct impact on the materials and packaging configurations that can be used.

In this chapter, we review heat transfer analysis for microwave and millimeter-wave electronic packages. We start with a few fundamental concepts related to thermal analysis. The first is amplifier efficiency and dissipated thermal power. Given an amplifier's bias conditions, it is important for the dissipated thermal power to be calculated. Because the goal of thermal analysis is to ensure that all devices will operate reliably, we also review the reliability of semiconductor devices. After a discussion of device junction temperature, a simple method for predicting the junction temperature of electronic components is presented. We conclude with a top-level review of the numerical methods used for thermal analysis.

9.1 Heat Transfer Mechanisms

Heat transfers from one area to another area due a temperature difference. Heat transfer is described using several different mechanisms. The first is conduction, which is heat transfer through a medium that is solid or a fluid that is stationary. The rate of heat transfer through a material in the x direction, for instance, per unit area perpendicular to the direction of heat transfer is referred to as the heat flux and is expressed as

$$q_x'' = k\frac{dT}{dx} \quad \mathrm{W/m^2} \tag{9.1}$$

where k is the thermal conductivity (W/mK) and dT/dx is the temperature gradient in the x direction. The thermal conductivity k is dependent on the type of material being used. For most practical materials, thermal conductivity varies as a function of temperature. However, in our analysis we will assume that it is temperature independent.

Thermal conductivity varies significantly for the various types of electronic packaging materials. Aluminum, for instance, has a thermal conductivity of approximately 220 W/mK. Alumina ceramic has a thermal conductivity of approximately 25 W/mK. LTCC ceramic has a thermal conductivity of approximately 2 W/mK. Plastic has a thermal conductivity of approximately 0.2 W/mK. The fact that the thermal conductivity of these materials varies by approximately progressive factors of 10 from each other makes it easy to remember and they are commonly used materials in microwave and millimeter-wave packaging.

As an example, consider a block of aluminum with $L = 10$ mm thick that is intimately connected to a motherboard. If the temperature at the interface between the motherboard and the aluminum is $T_1 = 50°\mathrm{C}$ and the temperature on the opposite side of the alumina is $T_2 = 48°\mathrm{C}$, calculate the heat flux. From (9.1), we know that

$$q_x'' = k\frac{dT}{dx} = k\frac{T1 - T2}{L} = 220\frac{W}{mK}\cdot\frac{(273+50)K - (273+48)K}{0.01m} = 44{,}000\frac{W}{m^2}$$

Heat also transfers due to convection when a surface and a moving fluid are at different temperatures. Convection occurs because of conduction (heat diffusion) and because of the macroscopic motion of the fluid (advection). The conduction portion of the heat transfer occurs near the surface of the solid material where the motion of the fluid varies from zero (at the solid surface) to the maximum fluid velocity at some distance from the solid surface. In this case the heat flux is given by

$$q'' = h(T_S - T_\infty) \quad W/m^2 \tag{9.2}$$

where:

h = convection heat transfer coefficient (W/m2K)

Ts = temperature at the surface of the solid (K)

T_∞ = fluid temperature (K)

The convection heat transfer coefficient, h, includes all of the physical contributions to the heat transfer such as the material parameters of the fluid, the surface treatment/geometry of the solid, and all associated transport mechanisms. In general, laminar flow of the liquid will result in a lower heat transfer coefficient, but turbulent flowing liquid will have a larger heat transfer coefficient. This is due to the fact that turbulent flowing liquid results in a thinner layer of stagnant fluid at the surface of the solid.

Heat also transfers due to radiation, energy that is emitted by matter. It is a result of radiation of electromagnetic waves from a material. In contrast to conduction or convection, radiation does not require a medium for the transfer of energy. Rather, radiation is most effective in a vacuum, void of any matter. The heat flux radiated at a material surface is given by

$$q'' = \varepsilon\sigma T_s^4 \quad \text{W}/\text{m}^2 \tag{9.3}$$

where:

ε = the emissivity of the surface ($0 \le \varepsilon \le 1$)
σ = the Stefan-Boltzmann constant (5.67×10^{-8} W/m2K4)
T_s = temperature of the surface (K)

The emissivity ε, of the radiating surface is a figure of merit for how efficient the surface is at emitting radiation compared to an ideal radiation of energy.

The majority of this chapter focuses on conduction heat transfer because it is the mechanism that is more often encountered for microwave and millimeter-wave packaging from the IC level to the module or motherboard level. Certainly, most motherboards and modules are connected to some type of heat sink, cold plate, or other heat transfer surface. However, for the purposes of this chapter, heat sinks and cold plates can be considered to be isothermal surfaces.

9.2 Amplifier Efficiency and Dissipated Thermal Power

Prior to detailed heat transfer analysis, it is important to understand the source of the heat in microwave and millimeter-wave packaging. The majority of the heat that is generated in electronic circuits is from the ICs used. Amplifiers are often the source of significant heat energy.

Amplifiers take an input signal and increase its amplitude. To do this, an amplifier requires electrical power, which is called the DC bias. Figure 9.1 il-

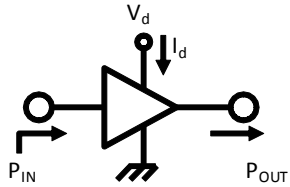

Figure 9.1 Schematic showing an amplifier input power (P_{IN}), output power (P_{OUT}), drain dias voltage (V_d), and drain bias current (I_d).

lustrates an amplifier with a bias voltage V_d and bias current I_d. The DC power into the amplifier is

$$P_{DC} = V_D \cdot I_D \quad \text{W} \tag{9.4}$$

where VD represents the DC bias voltage and ID the DC bias current.

The power added efficiency (PAE; expressed as a percentage) of an amplifier indicates how effective the amplifier is at converting the DC bias power into output power. In other words, it is a metric for how efficient the amplifier is in converting the bias power into output power, taking into account the input power. It is given by

$$PAE = \eta = \frac{P_{RFOUT} - P_{RFIN}}{P_{DC}} = \frac{P_{RFOUT} - P_{RFIN}}{V_D \cdot I_D} \tag{9.5}$$

where:

η = power added efficiency (PAE)
P_{rfOUT} = rf output power from the amplifier
P_{rfIN} = rf input power to the amplifier
PDC = DC power into the amplifier from the bias voltage and current.

PAE is usually expressed as a percentage so that (9.5) is normally multiplied by 100. A major activity for medium- and high-power amplifiers is the improvement of the PAE. This should be obvious since improved PAE means that less DC bias is required, which results in less power being dissipated and less power being required from the system power supply.

The important thing for thermal simulations is the amount of thermal power that is dissipated in the amplifier because this will be used in subsequent thermal calculations. The thermal power is just the DC input power minus the rf input power and rf output power. Therefore, the dissipated power in the amplifier is

$$P_{DISS} = P_{DC} + P_{rfIN} - P_{rfOUT} \quad \text{W} \tag{9.6}$$

By solving (9.2) for PDC and substituting into (9.3), we obtain

$$P_{DISS} = \frac{P_{rfOUT} - P_{rfIN}}{\eta} + P_{rfIN} - P_{rfOUT} \quad \text{W} \tag{9.7}$$

Using (9.6) or (9.7) we can determine the dissipated power for most amplifiers using data supplied by the manufacturer. Consider an amplifier that delivers an output power of 200 mW with an input power of 10 mW, a bias voltage of 5V, and a bias current of 200 mA. The DC power is

$$P_{DC} = 5\text{V} \times 0.2A = 1.0\,W$$

The power added efficiency is

$$\eta = \frac{P_{rfOUT} - P_{rfIN}}{P_{DC}} = \frac{0.2W - 0.01W}{1.0W} = 0.19\,or\,19\%$$

The power dissipated is

$$P_{DISS} = P_{DC} + P_{rfIN} - P_{rfOUT} = 1.0W + 0.01W - 0.2W = 0.81W$$

Therefore, the amplifier will dissipate 810 mW, which must be accommodated by the thermal design and material choices used for the packaging. However, it is important to understand how this dissipated power and, more importantly, the resulting junction temperature affect the reliability of the transistor.

9.3 Reliability and Arrhenius Equation

If the goal of a thermal design is to achieve a required level of reliability (i.e., operating lifetime of the device) given a device's dissipated power and junction temperature, then it is important to understand how the device junction temperature is related to the lifetime of the device. For most semiconductors operating lifetime is expressed in terms of mean time to failure (MTTF). The MTTF is determined by measuring the device lifetime at elevated temperatures. The results can be fitted to a curve, known as the Arrhenius curve, for extrapolation at lower temperatures. It is based on the Arrhenius equation, which gives the rate at which a failure will occur:

$$R = Ae^{(-E_a/kT)} \tag{9.8}$$

where:

R = rate at which the diffusion process occurs
A = scaling constant
E_a = activation energy
k = Boltzmann constant = 8.617×10^{-5} (eV/K)
T = temperature (K).

The mean time to failure is inversely proportional to the reaction rate. If we are able to measure the mean time to failure, MTTFH, at an elevated temperature, TH, and we want to know the mean time to failure, MTTFL, at a lower temperature, TL, then we have

$$MTTF_H \propto \frac{1}{R_H} = \frac{1}{A} e^{(E_a/kT_H)} \tag{9.9}$$

$$MTTF_L \propto \frac{1}{R_L} = \frac{1}{A} e^{(E_a/kT_L)} \tag{9.10}$$

If we divide (9.10) by (9.9) and solve for MTTFL, we obtain

$$MTTF_L = MTTF_H \exp\left[\frac{E_a}{k}\left(\frac{1}{T_L} - \frac{1}{T_H}\right)\right] \tag{9.11}$$

Often, (9.11) is referred to as the acceleration factor. As an example of its usefulness, consider the case of a semiconductor device that has a 500-hour lifetime at a junction test temperature of 160°C with an activation energy E_a of 0.7 eV. It is possible to find the lifetime if it is operated at a junction temperature of 60°C as follows:

$$\begin{aligned} \mathrm{MTTF_L} &= 1000\exp\left[\frac{0.7}{8.617\mathrm{x}10^{-5}}\left(\frac{1}{(273+60)} - \frac{1}{(273+160)}\right)\right] \\ &= 2.79\times10^5 \text{ hours} = 31.9 \text{ years} \end{aligned}$$

An illustration of an MTTF plot is shown in Figure 9.2. Typically, semiconductor devices are subjected to three or more elevated temperatures and the MTTF is determined at each temperature. This type of testing is referred to as accelerated life testing. The idea behind this test is that the failure mechanisms are dependent on time and temperature. If the MTTF is known at high temperatures, then the result can be extrapolated to lower temperatures. The result is plotted as a function of temperature as shown in Figure 9.2. A curve fit is used to obtain the activation energy or it can be calculated directly using the following equation:

$$E_a = \frac{k}{\log_{10}(e)} \frac{d\log_{10}(MTTF)}{d(1/T)} \quad \text{eV} \tag{9.12}$$

Each failure mechanism will have its own activation energy. Some types of failure mechanisms are diffusion, contamination, intermetallics, corrosion, and gate defects.

The required MTTF is determined by the application. Space-based applications and many military applications typically require 20-year or longer MTTFs. Commercial applications require somewhat less. For most applications, designers will add a safety factor to the MTTF requirement that can be

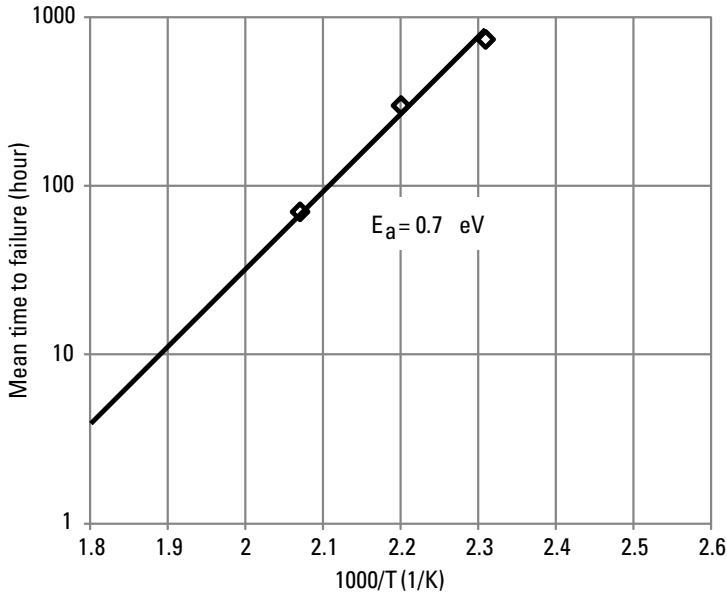

Figure 9.2 Plot of MTTF for a transistor with an activation energy of 0.7 eV with data obtained using accelerated life testing at high temperatures.

as high as a factor of 2. Once the MTTF is known, the maximum junction temperature can be calculated. Ensuring that the semiconductor junction never exceeds the maximum junction temperature becomes the goal of the thermal design.

9.4 Device Junction Temperature

The challenge for electronic packaging is to maintain a device junction temperature that is lower than the maximum allowed for the device. The majority of the time thermal analysis is centered on active devices such as integrated circuits, transistors, and diodes. However, some passive devices can dissipate enough thermal energy that they will need to be analyzed as well.

Most manufacturers of semiconductor devices will specify the thermal resistance between the junction of the device to the case of the device, θ_{jc}, and the maximum junction temperature. Consider the QFN package amplifier shown in Figure 9.3(a). The device mounted in the QFN is a GaAs MMIC amplifier mounted on a Cu die paddle. In this example, the device manufacturer supplies the thermal resistance from the junction of the device to the "case," θ_{jc}, which is equal to 2.3°C/W. The case is just the bottom of the Cu die paddle so that in this case, $T_{mount} = T_{case}$.

The path of the heat generated at the junction to the bottom of the die paddle goes through three different materials, each with its own thermal resistance. The junction-case thermal resistance is the combination of the thermal resistance of the GaAs semiconductor, epoxy used to attach the MMIC to the Cu paddle, and the Cu paddle as shown in Figure 9.3(b). For the vast majority of packaged dies, the designer will not have access to the details inside the package. Therefore, the designer will be concerned with the θ_{jc} supplied by the manufacturer. Given the dissipated power P_{DISS}, it is possible to determine the junction temperature:

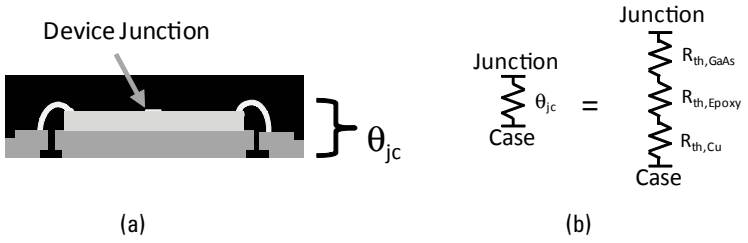

Figure 9.3 (a) Thermal resistance of a QFN package from the junction to the case. (b) The junction case thermal resistance is a combination of the internal thermal resistances.

$$\text{Junction Temp} = T_{\text{junction}} = T_{\text{mount}} + P_{DISS}\theta_{jc} \tag{9.13}$$

As an example, calculate the junction temperature of a 0.5W QFN packaged amplifier with a 20-dB gain, $\theta_{jc} = 12°C/W$, a bias voltage of 5V, and a bias current of 750 mA that is mounted on a motherboard at a temperature of 40°C.

Using (9.6) and ignoring the input power since the gain of the amplifier is 20 dB, we obtain

$$P_{DISS} = P_{DC} - P_{rfOUT} = 5V\,x\,0.75A - 0.5W = 2.75W$$

Therefore, the junction temperature can be found using (9.13) as

$$T_{junction} = T_{mount} + P_{DISS}\theta_{jc} = 40C + 2.75W\,x\,12C/W = 73°C$$

The manufacturer specifies that the maximum junction temperature must be below 125°C, so the junction temperature is likely acceptable.

9.5 Junction Temperature with Multiple Material Layers

The package into which the die/heat skin assembly is integrated may be constructed of many different materials with varying thicknesses and thermal conductivity. The thickness and conductivity are properties of the material selection, which is typically driven by transitions of the coefficient of thermal expansion (CTE). This is because the constraint of needing matched CTE materials increases the challenge of packaging. One of the main goals of heat transfer analysis of an IC within a package is to determine the junction temperature of the active devices. Consider the example of a GaN high-power amplifier

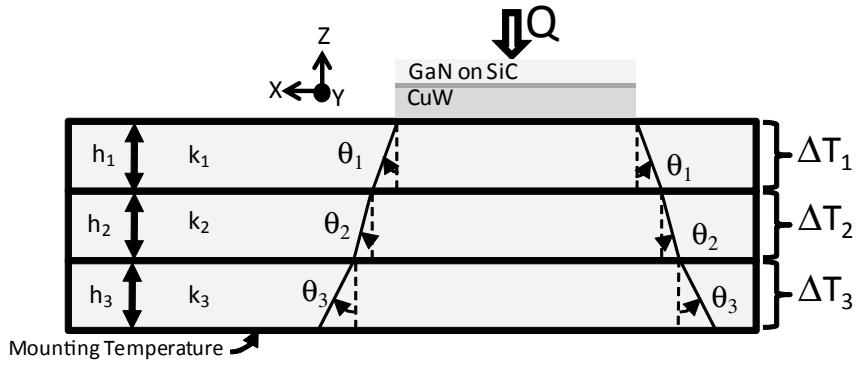

Figure 9.4 GaN amplifier integrated into a package with multiple material layers.

shown in Figure 9.4. The amplifier is shown mounted on a CuW heat sink with three layers of packaging material below it. These layers could be CuMo heat spreaders, high thermal conductivity epoxy, ceramic, or any other material. Also shown in the figure are the heat spreading angles, θi, where the subscript i is the layer number. The heat spreading angle is a useful concept for representing the fact that heat will spread differently depending on the properties of each layer. In general, higher thermal conductivity materials have a larger heat spreading angle.

The increase in the effective area of the heat source due to the spreading angle can be calculated by examining the geometry. The area of the heat source is increased relative to the area in the prior layer, as shown in Figure 9.5. The figure considers the *x* direction but the same analysis is true for the *y* direction assuming the layer is homogenous. From the figure it is recognized that

$$x_i = x_{i-1} + 2\Delta x_i = x_{i-1} + 2h_i \tan\theta_i \tag{9.14}$$

The temperature drop across each layer depends on the layer thickness, the heat entering each layer, and the thermal conductivity of the layer. The temperature drop can be calculated as

$$\Delta T_i = \frac{Qh_i}{k_i x_i y_i} = \frac{Qh_i}{k_i(x_{i-1} + 2h_i \tan\theta_i)(y_{i-1} + 2h_i \tan\theta_i)} \tag{9.15}$$

Or for the case with θi = 45 degrees,

$$\Delta T_i = \frac{Qh_i}{k_i(x_{i-1} + 2h_i)(y_{i-1} + 2h_i)} \tag{9.16}$$

where:

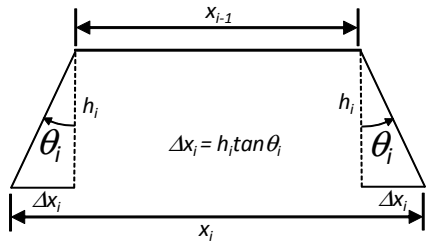

Figure 9.5 The heat is spread in each layer, which reduces the temperature drop.

k_i = thermal conductivity of the ith layer (W/mK)

Q = heat energy created (W)

h_i = thickness of the ith layer (m)

ΔT_i = temperature difference across the ith layer (K)

For the case with $\theta_i = 0$ degrees, there is no spreading and the area of the heat source is assumed to be the same through the material stack. This approximation can be considered a worst case one because ignoring spreading results in a higher estimation for the temperature drop in each layer and (9.15) reduces to

$$\Delta T_i = \frac{Qh_i}{k_i xy} \tag{9.17}$$

The use of (9.17) can be considered a first-order approximation to the thermal analysis. Other closed-form methods can be used, and extremely sophisticated analysis software exists that is able to accurately predict both steady-state and transient thermal effects.

Now, returning to the GaN high-power amplifier of Figure 9.4, we find from the datasheet for the amplifier that the thermal resistance from the junction to the bottom of the CuW heat spreader is 2.3°C/W. Also, we know from the datasheet that the amplifier will dissipate 38W of energy and that the size of the amplifier is 3.6 mm^2. The first layer in figure is high thermal conductivity epoxy with a thermal conductivity of TC_1 = 24 W/mK and a thickness of $h_1 = 0.01$ mm. The second layer is copper molybdenum (CuMo) with a thermal conductivity of TC_2 = 230 W/mK and a thickness of h_2 = 3.0 mm. The last layer is aluminum (Al) with a thermal conductivity of $TC_3 = 210$ W/mK and a thickness of h_3 = 2.0 mm. We can use (9.15) to calculate the temperature rise at each layer, and as a worst case simulation, the spreading angle was assumed to be zero. The temperature rise in each layer and the junction-to-case rise can be summed and added to the mounting temperature to determine the junction temperature of the amplifier. Figure 9.6 shows the results of the calculations.

$$\begin{aligned}&\text{Device Junction Temperature} = \\ &\text{Mounting Temp} + \Delta T_3 + \Delta T_2 + \Delta T_1 + T_{jc}\end{aligned} \tag{9.18}$$

$$= 40C + 27.92C + 38.24C + 6.11C + 87.4C = 199.67C$$

The datasheet shows that the device maximum junction temperature is 225°C so this analysis predicts reliable device operation. This analysis, however, uses several approximations and some effects are ignored. For instance, the heat

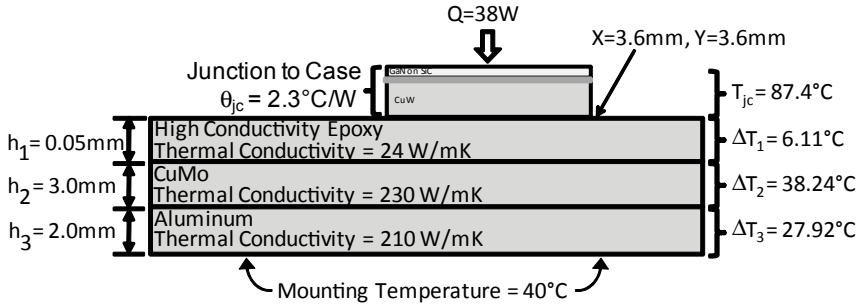

Figure 9.6 Temperature across each layer.

spreading is assumed to be zero, the thermal resistance at the junctions between materials is assumed to be zero, the mounting surface is assumed to be an isotherm, and interface materials will likely be needed in a practical realization. It is common practice to have a liquid heat exchanger as a mounting surface, and the high heat flux means the mounting temperature can vary significantly local to the electronics, adding considerable complexity to the simplified boundary condition provided in Figure 9.6. Even with these approximations, this analysis approach, when applied with care, can yield approximations that can act as a starting point for a detailed thermal analysis.

A software program has been written by the author implementing the thermal analysis method outlined in this section. It is described in Appendix C.

For many designs, numerical heat transfer analysis will be conducted. Most thermal numerical analysis techniques are based on finite difference, control volume, finite element, and other hybrid methods.

9.6 Thermal Simulations Using Spice

Spice is a familiar simulation tool for many engineers, especially electrical engineers. It was developed for the purpose of performing transient modeling of electrical circuits. The familiarity of Spice and the fact that it has been integrated into many of the commercially available microwave circuit simulators make it attractive as a simulation platform for thermal modeling [1].

This approach is based on the analogies between heat transfer and electrical circuit modeling. Heat flow can be modeled as electrical current, thermal resistivity can be modeled as electrical resistivity, and thermal capacity (thermal mass) can be modeled as electrical capacitance. If these analogies are applied, then the predicted voltages in the circuit can be interpreted as temperatures at the material interfaces.

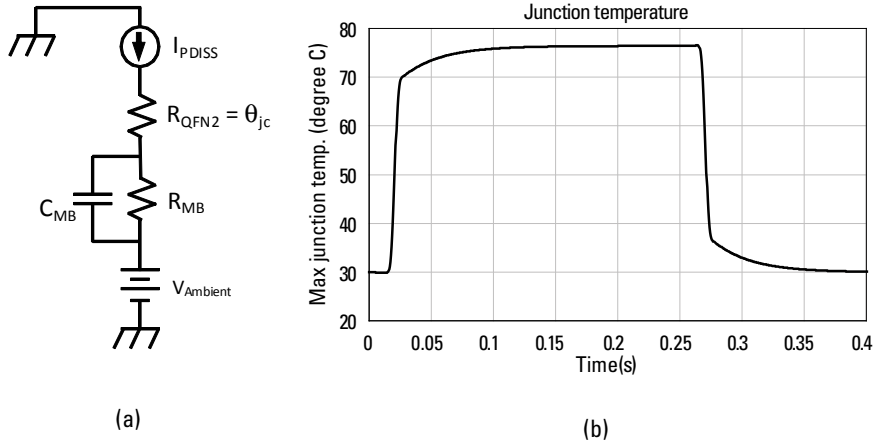

Figure 9.7 Electric circuit model for thermal analysis showing (a) the thermal model schematic, and (b) the simulated junction temperature as a function of time.

A simplified spice model for a QFN mounted to a motherboard and heat sink is shown in Figure 9.7(a). The dissipated power is represented as a current source such that every watt of power dissipated is equal to one amp of current from P_{DISS}. As an example, consider an LNA with a bias voltage of 5V and a current of 160 mA that dissipates 0.8W so the current, I_{PDISS}, is 0.8A. The manufacturer datasheet for the LNA gives the θ_{jc} as 48°C/W, which is represented in the schematic as the thermal resistance, R_{QFN2}. The motherboard has a thermal capacity, C_{MB}, of 0.003 W•s/°C and thermal resistance, R_{MB}, of 10°C/W. Finally, the motherboard is connected to a heat sink at an ambient temperature of 30°C. The heat sink is shown in Figure 9.7 as a DC bias, $V_{Ambient}$. Circuit simulation determined that the junction temperature for a constant thermal dissipation is 76.4°C. Figure 9.7(b) shows the transient response to a pulsed heat source. The results show that the thermal rise time is about 0.1s.

The correlation between thermal simulation and electric circuit simulation can be seen by examining Table 9.1. The table will help with translating thermal parameters into the parameters needed for electrical stimulation.

9.7 Thermal Simulation Using the Finite Difference Method

As with electromagnetic numerical simulations, heat transfer numerical simulations divide the solution structure into a mesh. The temperature is determined for each point in the mesh. For heat transfer problems, the finite difference method is commonly used. The heat equation is given by [2]

Table 9.1
Comparison of the Units Used for Heat Transfer Simulation in Spice Simulators

Parameter Type	Units for Heat Transfer	Units in the Circuit Simulator
Thermal resistance	°C/W	Ohms
Thermal mass	J/°C	Farads
Dissipated power	Watts	Amps
Temperature	°C	Volts

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)+\dot{q}=\rho c_{SH}\frac{\partial T}{\partial t} \tag{9.19}$$

where:

T = temperature distribution T(x,y,z)
$\dot{q}$ = rate of energy generated per unit volume (W/m3)
ρ = density (kg/m^3)
c_{SH} = specific heat (J/kgK).

The heat equation provides the temperature distribution in a 3D volume as a function of time. It also obeys the conservation of energy law. If the thermal conductivity is a constant, steady-state condition, and there is no energy generation, then the 2D version of the heat equation can be simplified to

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}=0 \tag{9.20}$$

For a grid with m elements in the x direction and n elements in the y direction, the internal node at m,n can be approximated by

$$\left.\frac{\partial^2 T}{\partial x^2}\right|_{m,n}\approx\frac{\partial T/\partial x\big|_{m+1/2,n}-\partial T/\partial x\big|_{m-1/2,n}}{\Delta x} \tag{9.21}$$

This equation gives the x dependent temperature at the mth, nth node in the mesh. Next, the temperature gradients need to be determined. They are given by

$$\left.\frac{\partial T}{\partial x}\right|_{m+1/2,n} \approx \frac{T_{m+1,n} - T_{m,n}}{\Delta x} \tag{9.22}$$

$$\left.\frac{\partial T}{\partial x}\right|_{m-1/2,n} \approx \frac{T_{m,n} - T_{m-1,n}}{\Delta x} \tag{9.23}$$

Substituting (9.22) and (9.23) into (9.21), we obtain

$$\left.\frac{\partial^2 T}{\partial x^2}\right|_{m,n} \approx \frac{T_{m+1,n} + T_{m-1,n} - 2T_{m,n}}{(\Delta x)^2} \tag{9.24}$$

Using the same procedure for the y direction, we can show that

$$\left.\frac{\partial^2 T}{\partial y^2}\right|_{m,n} \approx \frac{\partial T/\partial y|_{m,n+1/2} - \partial T/\partial y|_{m,n-1/2}}{\Delta y} \approx \frac{T_{m,n+1} + T_{m,n-1} - 2T_{m,n}}{(\Delta y)^2} \tag{9.25}$$

If the mesh is chosen so that $\Delta x = \Delta y$, and if (9.25) and (9.24) are substituted into (9.20), we obtain

$$T_{m,n+1} + T_{m,n-1} + T_{m_1,n} + T_{m-1,n} - 4T_{m,n} = 0 \tag{9.26}$$

The result is that the heat equation can be reduced to an algebraic approximation that is valid for any interior node that is equal distance from its four adjacent nodes. Note that it is possible to generate finite difference equations for nodes that are not interior such as edges, corners, or near a curved surface [3].

The solution to (9.26) and the determination of the temperature distribution require the development of a mesh, application of the correct difference equation for each node, and the solution of a set of linear equations using matrix inversion. The finite difference method has been implemented in commercially available software.

Many other numerical methods have been used and some have been implemented in commercially available software. For instance, the finite element method is used extensively and has been implemented in commercially available software.

9.8 Conclusions

Heat transfer analysis is an important part of electronic packaging. Due to the large heat flux that exists in microwave and millimeter-wave packaging, this problem is especially important. The thermal goal of an electronic package is to maintain a junction temperature that will achieve the required lifetime of the electronics. Normally, elevated temperature testing is conducted to determine the MTTF for the devices. This results in a junction temperature requirement. Using the bias conditions of an amplifier, the dissipated power and the junction temperature can be determined. For most designs, commercially available software tools will be used to analyze heat transfer.

Questions

1. If an MMIC with dimensions of 3 mm × 3 mm that dissipates 3W of power is mounted onto an alumina substrate that is 1 mm thick and the temperature at the die-alumina interface is 80°C, what is the temperature on the bottom side of the alumina?
2. A liquid cooling system consisting of a metal cold plate with coolant flowing inside is used to cool electronics that dissipate a heat flux of 10 W/m^2. If the temperature of the fluid is 60°C and the temperature of that interface between the coolant and metal cold plat is 90°C, what is the coefficient of convective heat transfer?
3. If an electronic package at a temperature of 80°C that is part of a satellite system must use radiation as part of its thermal management design, what is its emissivity?
4. What is the power added efficiency (expressed in percentage) of a high-power amplifier with an output power of 2W at a bias of 12V and 700 mA with an input power of 0.05W? What is its dissipated power?
5. Derive (9.12) from (9.11).
6. What is the mean time to failure (MTTF) for a device operating at 100°C if it has an activation energy of 0.7 eV and if the MTTF at 203°C is 100 hours?
7. If a set of high-temperature life tests shows that the mean time to failure for a junction temperature of 227°C is 10 hours, at 203°C it is 40 hours, and at 161°C it is 500 hours, what is the activation energy? What is the expected lifetime for a junction temperature of 125°C? Would you consider this device to be reliable if operated at 125°C and

why or why not? At what temperature should this device be operated to be considered reliable for most commercial applications?

8. What is the junction temperature of a low-noise amplifier in a three-pin SOT-89 package that has a junction-to-case thermal resistance of 34°C/W if the amplifier is operating at a bias of 5V at 130 mA?
9. What is the junction temperature of a 3.5-mm × 3.5-mm GaN Ku Band MMIC amplifier with high gain and with an output power of 10W operating with a bias of 12V at 2A. Its junction-to-case thermal resistance is 2.9 W/mK and it is mounted directly (neglect the attachment material) on a single layer of aluminum nitride ceramic (k = 160 W/mK) that is 1.5 mm thick. Assume that the bottom of the aluminum nitride is connected directly to a 30°C cold plate.
10. Repeat Question 9, except add a layer of attachment material between the MMIC and aluminum nitride that is 0.05 mm thick. Generate a plot showing the MMIC junction temperature as a function of the thermal conductivity of the attachment material. Assume that the thermal conductivity of the attachment material varies from 1 to 100 W/mK.
11. Repeat Question10, except assume that the attachment material is a high thermal conductivity epoxy with a thermal conductivity of 25 W/mK and assume that the cold plate is aluminum that is 2 mm thick and that 30°C liquid cooling is below the aluminum. Plot the junction temperature of the MMIC as a function of the convection heat transfer coefficient.
12. Perform the heat transfer analysis shown in Figure 9.6 assuming a heat spreading angle of 45 degrees. Using the resulting junction temperature prediction, what would the lifetime be assuming the MTTF curve shown in Figure 9.2?
13. Using a circuit simulator, generate a transient plot of the junction temperature of an MMIC amplifier that has a thermal resistance of 15°C/W, is dissipating 0.15W, and is mounted to a motherboard with a thermal resistance of 15C/W and a thermal capacity of 0.004 W•s/C connected to a heat sink at 25°C. From the plot determine the time it takes to reach thermal steady state.

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10

Electromagnetic Modeling

For low-frequency packaging, electromagnetic (EM) modeling is rarely used. This is because the electrical design concerns at low frequency are different. However, it is used extensively for microwave and millimeter-wave electronic packaging because EM modeling can capture the effects of the physical design and materials on the electrical performance. This, in turn, allows for optimization of the packaging to achieve the desired performance goals.

In general, the goal of EM simulations is to solve the electric and magnetic fields of a structure and generate useful information such as scattering parameters, radiation patterns, electric field strength, or some other output. The output is then used as part of a circuit simulation, as input to generate an equivalent circuit model, or as part of an optimization of the structure being analyzed. The EM simulator actually solves Maxwell's equations for the structure. Those equations are:

$$\nabla \times \bar{E} = \mu \frac{\partial \bar{H}}{\partial t} \tag{10.1a}$$

$$\nabla \times \bar{H} = \varepsilon \frac{\partial \bar{E}}{\partial t} \tag{10.1b}$$

$$\nabla \cdot \bar{D} = \frac{\rho}{\varepsilon_0} \tag{10.1c}$$

$$\nabla \cdot \overline{B} = 0 \tag{10.1d}$$

Many different numerical methods have been developed to solve Maxwell's equations and all of them divide the structure to be analyzed into a mesh. Then, Maxwell's equations are solved for each section of the mesh. Some analysis methods use volume meshing to create a mesh for the complete 3D volume of the structure. The benefit of this approach is that nearly any arbitrary 3D structure can be created, meshed, and then analyzed. The volume meshing approach is useful for circuits with nonplanar structures such as wire bonds and circuit transitions with features in three dimensions. The drawback of volume meshing is that a volume has a large number of mesh elements so it can be time consuming to achieve a solution. Other types of EM simulators use a planar mesh. This approach is commonly used for planar circuits such as microstrip, stripline, CPW, and CBCPW to name just a few. In general, planar simulators provide solution results faster than volume meshing simulators will for planar circuits. However, planar simulators cannot analyze circuits with arbitrary 3D features such as wire bonds. Therefore, a trade-off must be made and the engineer will need to know when to use a volume mesh or planar mesh EM analysis.

Prior to the debut of commercial EM simulators, it was common for microwave and millimeter-wave circuits to require several iterations of design-fabricate-test before an acceptable result was obtained. The savviest designers were able to write their own custom EM analysis. Although custom software is still being written that implements one of the well-understood methods [1], several such types of software have been implemented in commercially available EM simulators. For most applications, it is efficient to use them rather than writing custom software. Furthermore, enormous effort has gone into the improvement of commercial EM simulators since their debut in about 1989 [2]. The result is highly sophisticated EM simulators that can analyze and optimize a structure in a number of hours compared to the many weeks of the design-fabricate-test cycle that used to be common. Another consequence of the advent of commercial EM simulators is that the cost of development and time to market for new products has been reduced dramatically.

Most of the commercially available EM simulators follow the same general procedure for the problem setup as that shown in Figure 10.1. The first step is to define the enclosure, which contains the circuits to be analyzed, and then either draw the circuit features or import them from another application. The second step is to define the materials for the dielectric, metal, and other materials that comprise the structure to be analyzed. The third step is to define the boundary conditions such as radiating or absorbing boundaries. The fourth step is to set up the ports to be analyzed. The port setup procedure is usually very straightforward, although some port setups can be more elaborate. It is important to properly define the ports prior to attempting the EM analysis

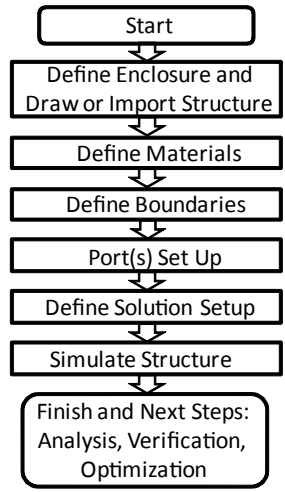

Figure 10.1 Typical process flow for problem setup for most EM simulators.

since the simulator needs to know how to inject the signals used during the simulation. The fifth step is to set up the solution parameters such as frequency range and step size. The last step is to analyze the structure, which may include optimization if the commercial EM tool being used supports this capability. Although there are major differences among the commercially available EM simulation tools, they generally follow these same process steps for setting up problems for solution.

After this procedure has been completed, the results are examined to verify that they make sense. It is important not to blindly accept the results of any simulation because the problem may have been set up improperly, for example, the structure may have been incorrectly defined or the material type incorrectly specified. Also, the program can yield an incorrect result based on the way the problem was defined. Often, these types of issues can be uncovered immediately by just applying a few simple checks. Checking the results of EM simulators is important so that designers can be confident that the predictions from a simulator will agree with the measured data for the same structure.

As with most analysis software, the result will not be accurate if the model is not accurate. Therefore, it is important to properly set up the model and the ports. If the problem is not properly configured, some EM simulators will give nonphysical results. That is, the results can violate the conservation of energy law. The conservation of energy law states that the total amount of energy coming out of the passive structure being analyzed must not be greater than the energy that is put into it. In other words, for a passive two-port structure,

$$|S11|^2 + |S21|^2 \leq 1 \tag{10.2}$$

$$|S12|^2 + |S22|^2 \leq 1 \tag{10.3}$$

In the ideal case where the structure is completely lossless and has zero radiation, (10.2) and (10.3) will be equal to unity. These equations are useful for checking EM simulation results because if they are violated, it may well be that there are problems with the structure, materials, or the definition of the ports. Improperly defined ports are a common reason why an EM simulator will generate nonphysical results.

Another practical method for confirming that EM simulator results are valid is to verify that the port impedance that the simulator calculates is in the range that is expected based on transmission line formulas or a transmission line calculator. That is, for most problems, the transmission lines in the structures contacting the ports will be designed (dimensions and features) using a transmission line analysis tool. Always verify that the EM simulator predicted port impedance agrees (within acceptable tolerance).

The port field plot, if available in your EM simulator, is another check that can be performed to increase confidence in the results. In the majority of packaging simulations, transmission lines will be connected to the ports of an EM simulation. The designer must be familiar with the expected electric field plot for the transmission lines being used. This allows the designer to verify that the electric field of the port is indeed the expected field. This is important because the EM simulator may solve for a mode at the port that is not desired and that will not be excited in the actual physical circuit. Or, it may be that the simulator will capture a mode that the designer should be concerned about but did not initially see as an issue. In either case, checking the electric field plot at the ports will give the designer confidence that the results of the simulation are correct or instead give the designer some indication of possible issues with the design.

Often, to increase confidence in the results of EM simulations, designers will simulate the same structure using two different simulators. This is especially true for designs that are particularly critical (due to the budget or schedule) or for new design types for which prior experience does not exist. Moreover, some designers simulate their designs in two different simulators as a standard practice. It is best to use EM simulators based on very different analysis methods such as the finite element method (FEM), method of moments (MoM), or finite difference time domain (FDTD) method. If similar results are obtained from very different EM simulator tools, then it is possible to have a high degree of confidence that the simulation results are accurately capturing the physical effects.

The first portion of this chapter reviews, at a very high level, the fundamental theory behind the methods used by most commercial EM simulators. Some methods are more appropriate for a particular class of problems while

others are more generalized. For instance, the mode matching method is well suited for analysis of waveguide problems, whereas the MoM is most appropriate for wire antennas or planar circuits such as microstrip or stripline. Understanding the strengths and weaknesses of each method provides some insight so that one is able to choose the most appropriate simulator for the class of problem being analyzed. The final section addresses integrated analysis methods; for example, full physics-based analysis techniques that include EM, thermal, and mechanical analysis coupled together. The last section reviews the domain decomposition method (DDM), which divides a physical problem into regions that are solved using the most efficient method. A particular advantage of the DDM is that it is able to efficiently solve electrically large problems (problems that have a size of 100 wavelengths or more).

Field simulators that solve for currents in two dimensions but solve the fields in a 3D structure are often called 2.5D simulators. For this reason, MoM solutions are often referred to as 2.5D simulators and use planar mesh methods. If vertical currents in vias are correctly accounted for, then the solution is often referred to as 3D planar [2]. This is opposed to simulators that solve Maxwell's equations in three dimensions for any arbitrary structure (not only planar) and are therefore called 3D simulators. These simulators use volume mesh techniques.

10.1 Quasistatic Simulation of Transmission Lines

Though commercially available transmission line calculators are available, sometimes it is necessary to determine the line impedance and effective dielectric constant for transmission lines that are not included in the available software. In these cases, it can be useful to perform a quick simulation using a quasistatic method. This software can also be useful in obtaining a starting point for the physical dimensions for nontraditional transmission lines prior to full-wave simulations. A useful method is based on the variational method developed by Bhat and Koul [3], who generated a capacitance equation:

$$C = \frac{Z1}{Z2} \tag{10.4}$$

$$Z1 = \left[\int_{(c-W)/2}^{(c+W)/2} \frac{1}{W} \left\{ 1 + A \left| \left(\frac{2}{W} \right) \left(x - \frac{c}{2} \right) \right|^3 \right\} dx \right]^2 \tag{10.5}$$

$$Z2 = \sum_{n=1}^{\infty} \left[\left[\frac{2}{\left(n\pi YW^2 \right)} \right] \right] \left[\int_{(c-W)/2}^{(c+W)/2} \left\{ 1 + A \left| \left(\frac{2}{W} \right) \left(x - \frac{c}{2} \right) \right|^3 \right\} \sin\left(n\pi x / c \right) dx \right]^2 \tag{10.6}$$

By combining (10.5) and (10.6) into (10.4), solving the integrals, and simplifying, we obtain

$$C = \left[\left(1 + 0.25A \right)^2 \right] \Big/ \left[\sum_{n=1}^{\infty} \left[2 / \left(n\pi YW^2 \right] I_n^2 \right] \right. \tag{10.7}$$

where:

$$I_n = \int_{(c-W)/2}^{(c+W)/2} \sin(n\pi x/c) dx + \left(8A / W^3 \right) \int_{(c-W)/2}^{(c+W)/2} \left| x - c/2 \right|^3 \sin\left(n\pi/c \right) dx$$

$$= \left(\frac{2c}{n\pi} \right) \sin\left(\frac{n\pi}{2} \right) \left[\begin{array}{l} \sin\left(\dfrac{\beta_n W}{2} \right) \\ \\ + A \left(\dfrac{2}{\beta_n W} \right)^3 \left\{ \begin{array}{l} 3 \left[\left(\dfrac{\beta_n W}{c} \right)^2 - 2 \right] \cos\left(\dfrac{\beta_n W}{2} \right) \\ + \left(\dfrac{\beta_n W}{2} \right) \\ \left[\left(\dfrac{\beta_n W}{2} \right)^2 - 6 \right] \sin\left(\dfrac{\beta_n W}{2} \right) + 6 \end{array} \right\} \end{array} \right] \tag{10.8}$$

where:

$\beta_n = n\pi/c$

C = the line capacitance

c = width of the cavity that encloses the transmission line (see Figure 10.2)

W = width of the signal line (see Figure 10.2)

Y = the admittance of the transmission line = $Y2 + Y3$ (see Figure 10.2).

Substituting (10.8) into (10.7) and noting that $\sin(n\pi/2)$ in (10.8) is zero for all even values of n including $n = 0$, we can show that

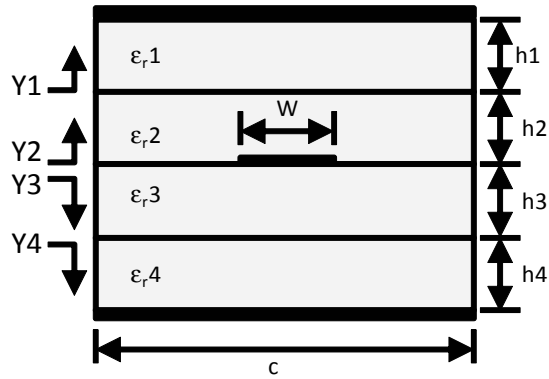

Figure 10.2 Transmission line with a single strip sandwiched between four dielectric layers with an admittance of $Y2 + Y3$.

$$C = \frac{\left[\left((1+0.25A)\right)^2\right]}{\sum_{n=odd}\left(L_n + AM_m\right)^2 P_n / Y} \tag{10.9}$$

where:

$$L_n = \sin\left(\beta_n W/2\right) \tag{10.10}$$

$$\mathrm{M_n} = \left(\frac{2}{\beta_\mathrm{n}\mathrm{W}}\right)^3 \left[\begin{array}{l} 3\left\{\left(\frac{\beta_\mathrm{n}\mathrm{W}}{2}\right)^2 - 2\right\}\cos\left(\frac{\beta_\mathrm{n}\mathrm{W}}{2}\right) \\ +\left(\frac{\beta_\mathrm{n}\mathrm{W}}{2}\right)\left\{\left(\frac{\beta_\mathrm{n}\mathrm{W}}{2}\right)^2 - 6\right\}\sin\left(\frac{\beta_\mathrm{n}\mathrm{W}}{2}\right) + 6 \end{array}\right] \tag{10.11}$$

$$P_n = \left(\frac{2}{n\pi}\right)\left(\frac{2}{\beta_n W}\right)^2 \tag{10.12}$$

To determine the constant A in (10.9), simply maximize C relative to A by differentiating with respect to A and setting it equal to zero. Therefore, by solving for $\partial C/\partial A = 0$, we can show that

$$A = -\left[\frac{\sum_{n=odd} \frac{(L_n - 4M_n)L_n P_n}{Y}}{\sum_{n=odd} \frac{(L_n - 4M_n)M_n P_n}{Y}}\right] \tag{10.13}$$

For the transmission line shown in Figure 10.2, the admittance of the transmission line is shown to be $Y2 + Y3$ at the reference point of the signal line. The admittance ca-n be found as

$$Y = Y2 + Y3 \tag{10.14}$$

where:

$$Y1 = \varepsilon_0 \varepsilon_{r1}\left(\frac{1}{\tanh \beta_n h1}\right) \tag{10.15}$$

$$Y2 = \varepsilon_0 \varepsilon_{r2} \frac{Y1 + \varepsilon_0 \varepsilon_{r2} \tanh \beta_n h2}{\varepsilon_0 \varepsilon_{r2} + Y1 \tanh \beta_n h2} \tag{10.16}$$

$$Y3 = \varepsilon_0 \varepsilon_{r3} \frac{Y4 + \varepsilon_0 \varepsilon_{r3} \tanh \beta_n h3}{\varepsilon_0 \varepsilon_{r3} + Y4 \tanh \beta_n h3} \tag{10.17}$$

$$Y4 = \varepsilon_0 \varepsilon_{r4}\left(\frac{1}{\tanh \beta_n h4}\right) \tag{10.18}$$

This method was implemented in a software program with a user interface. The software is described in Appendix B. One benefit of this method is that once the algorithm has been implemented, changing to a different transmission line type simply requires the modification of the admittance for the particular transmission line of interest. In addition to single strip lines, this method can be applied to edge coupled and broadside coupled transmission lines.

10.2 Method of Moments

A popular implementation of the MoM is to use the Galerkin technique, which uses equivalent basis and testing functions and the result is known to be variational [4, 5]. The MoM has been applied in several different commercially available software programs and is popular for wire antennas and planar transmission line circuits such as microstrip. These MoM-based simulators can solve planar circuits for any arbitrary metal pattern in a multilayer dielectric structure such as an MMIC, ceramic substrate such as LTCC, or a laminate motherboard. For instance, this method can handle circuits with multiple dielectric layers with surface transmission lines, buried ground planes, buried bias lines, and buried transmission lines.

For planar circuit problems, the analysis assumes that the circuit is enclosed in a conducting rectangular box, as shown in Figure 10.3. The box can be treated as a rectangular waveguide supporting TE (transverse electric) and TM (transverse magnetic) waves in the dielectric region. It is possible to sum of all the modes in each dielectric region to match the tangential fields at the interface between the regions at $z = h$.

The task at hand is to determine the voltage on one subsection, which results from current on the other subsections (source-field pair). The planar circuit conductors are subdivided into N subsections and a current distribution for each subsection is assumed. The magnitude of the current in all of the subsections is varied to achieve a total tangential electric field of zero on all conductors. An $N \times N$ matrix is created in which each element represents the impedance with current and voltage vectors, such that

$$\bar{V} = \bar{\bar{Z}}\bar{J} \tag{10.19}$$

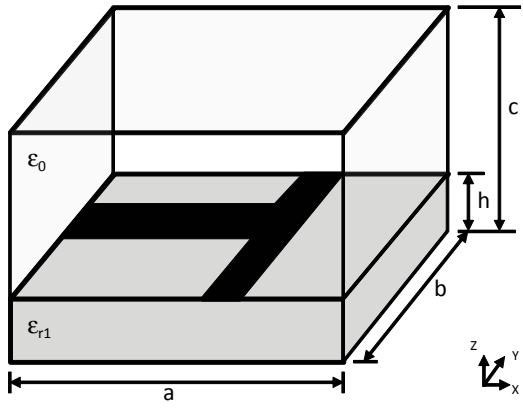

Figure 10.3 A simple microstrip circuit enclosed in a conducting box.

For MoM solutions, the inversion of the Z matrix requires the most computational effort and goes as N3 [6]. Once the currents on the surfaces of the planar metal conductors are known, then the scattering matrix or radiated field can be directly calculated.

10.3 Finite Element Method

FEM simulators use a volume meshing technique to solve Maxwell's equations so they can solve arbitrary 2D or 3D structures and circuits. Often, FEM is implemented in the frequency domain. Because FEM is a volume meshing technique, it is very common for a tetrahedron to be used as the basic shape in the mesh. This allows arbitrarily shaped 3D structures to be modeled. For instance, a tetrahedron can be combined to conform to the shape of a round wire bond that stretches from an IC to a bond pad. It is important for the mesh to be fine in locations where the fields are changing rapidly around 3D elements. At the same time, it is important for the mesh not to be overly complex for regions with little or no field. Therefore, many commercially available FEM simulators use adaptive meshing to create an optimum mesh. This is accomplished by calculating the error in the field at each element (tetrahedron). Those elements with the largest error are subdivided into smaller tetrahedrons. An iterative solution procedure is then implemented so that with each solution, the mesh is further refined until the desired accuracy is obtained. In this fashion, an optimal mesh can be created such that tetrahedrons are very dense in areas with small features and strong fields and there are fewer tetrahedrons in areas with weaker fields. The result ensures an accurate field, which means accurate performance predictions.

10.4 Finite Difference Time Domain Method

Although most EM simulation methods are performed in the frequency domain, the FDTD method solves Maxwell's equations in the time domain. The solution starts with Maxwell's curl equations, (10.1a) and (10.1b), and a mesh of nodal points is created. The electric and magnetic field components are imposed at particular places in space. The solution is carried out in the time domain using a discrete time step algorithm. The result is a transient time domain solution that is converted to the frequency domain using a Fourier transform [7]. One of the benefits of the FDTD method is that it is able to solve large structures with periodic features such as antenna arrays.

Fundamental numerical accuracy limitations inherent to the traditional FDTD method set the maximum time step size that can used in the analysis. In other words, structures with small features compared to a wavelength require

the use of a small time step size, which increases the solution time. To address this, the alternative direction implicit (ADI) method has been developed [8], which also provides unconditional numerical stability.

10.5 Mode Matching Technique

The mode matching technique is useful when the structure being analyzed has two (or more) regions in which Maxwell's equations are exactly known except at the boundary between the regions. The solution progresses by expanding the normal (orthogonal) fields in the regions, matching them at the interface, and solving for the modal coefficients. Because an infinite number of modes can exist, a convergence criterion must be established. Normally, a parameter of interest such as the scattering matrix value is plotted as a function of the number of fields being used in the solution. Once the variation in the parameter value is below the required accuracy, the solution is considered converged and the number of modes being considered is truncated [1].

The mode matching method is well suited for waveguide problems, but can also be used for microstrip and other transmission line types [9, 10].

10.6 Integrated Methods

EM simulation is used in an integrated fashion with other design software and this trend is increasing. For instance, it is now commonplace for microwave circuit simulators to be capable of fully integrating EM simulation results with circuit simulation such as linear frequency domain and harmonic balance simulations. This approach is especially helpful in the design of MMICs, modules, and motherboards. It is useful because the designer is able to select portions of the design that have features that are of particular concern such as possible coupling between sections of the circuit. These sections can be imported into the EM simulator and the results can be used directly in the circuit simulation. The intimate connection between the schematic, layout, and EM simulation now allows for complex designs (with active and passive circuits) to be more rapidly and accurately simulated.

A completely different level of simulator integration is the integration of EM simulation with circuit, thermal, and mechanical simulation. For many circuits, the thermal performance of an active circuit such as a MMIC depends on its thermal performance. Instead of having multiple analysis tools performing the analysis and then the designers translating results between them, the designer needs to have an integrated solution. For instance, thermal simulation results obtained from a thermal simulation tool must be translated into an MMIC design so that its performance, which is dependent on the junction

temperature of the device, can be determined. The results are then translated to a module or motherboard-level simulation to determine the impact on the system. If modifications to the motherboard are made as a result of the simulations, then new thermal simulations must be performed. This process is inefficient. Fully integrated solutions are required.

10.7 Domain Decomposition Methods

The domain decomposition method is a type of integrated simulation environment. In this approach, the EM simulator is an integrated simulation environment that contains several EM analysis methods. The EM simulator automatically selects the optimum simulation method for the various parts of the structure and fully integrates the results at the interface boundaries to create an integrated result [11]. A packaging example of how this approach may be particularly helpful is for modules with MMICs that are optimally analyzed by the MoM. The package is best analyzed using the FEM or FDTD method. In such a case, the simulation tool is fully integrated with multiple solution engines that are automatically and optimally applied to generate a result.

Questions

1. Why is it important to define the ports during the electromagnetic analysis process?
2. What is one common cause for EM simulators giving results that violate the conservation of energy?
3. Give at least three methods that can be used to verify that the results of an EM simulator are correct. Keep in mind that these methods are just a check of the EM simulation results and can help to identify possible issues with the model design or port setup.
4. If they are available, why is it helpful to use multiple EM simulators to analyze the same structure?
5. What is the difference between 2D, 2.5D, and 3D EM simulators?
6. When is it appropriate to use a 2.5D EM simulator? When is it not appropriate to use a 2.5D EM simulator?
7. Using the software described in Appendix B, generate a curve of line impedance versus line width (from 0.1 to 1.25 mm) for a suspended substrate stripline where $\varepsilon_{r1} = \varepsilon_{r3} = \varepsilon_{r4} = 0$, $\varepsilon_{r2} = 2.2$, $c = 4$ mm, $h1 = 0.5$ mm, $h2 = 0.127$ mm, $h3 = 0.25$ mm, and $h4 = 0.25$ mm.

8. What are the main differences between the MoM and FEM methods?
9. What is the domain decomposition method and how is it useful?

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11

Conclusions and Future Horizons

Electronic packaging at microwave and millimeter-wave frequencies has challenges that do not exist for packaging of low-frequency and DC products. As discussed in this book, one of the fundamental reasons for this is that the physical features of the packaging elements are an appreciable fraction of a wavelength. This causes packaging to perform differently at high frequencies. Also, we saw that the heat flux in ICs at high frequencies is much higher. This puts additional demands on the thermal management of the packaging and the system. As we demonstrated, interconnects such as wire bonds, ribbon bonds, and flip chips perform differently at microwave and millimeter-wave frequencies than they do at lower frequencies. This requires extensive modeling and simulation of interconnects, which is not necessary for lower frequency applications. Furthermore, we demonstrated that care must be taken with transitions between signal transport structures. This is not a concern for lower frequency applications, but must be taken into account when designing packages for use at high frequencies. These unique challenges at microwave and millimeter-wave frequencies require the design engineer to have training and expertise that is not needed for lower frequency package design.

The electronic packaging designer must have training and skill in the field of electromagnetics in order to properly understand and account for many of the unique challenges encountered. Because of the high heat flux, the package designer must also understand heat transfer. Careful selection of materials is required so that the signals are not degraded and the thermal management requirements are achieved. In short, the packaging engineer for microwave and millimeter-wave applications must be cross-trained in multiple disciplines.

What follows are 10 keys to successful electronic package development, followed by an assessment of the future of microwave packaging product development. It is argued that at microwave frequencies, products and services

are becoming commodity items. The chapter concludes with an assessment of packaging at millimeter-wave frequencies. It is argued that the availability of low-cost SiGe and Si CMOS processes have made millimeter-wave ICs affordable. This has put pressure on the electronic packaging design to enable low-cost products. The result is that new technology will come online enabling the development of high-data-rate communication systems that are low cost.

11.1 The 10 Keys to Successful Packaging

The 10 keys to successful electronic packaging at microwave and millimeter-wave frequencies are a type of process outline that, if followed, can improve the likelihood of meeting requirements with the first release. These items can also form a type of top-level checklist for product design reviews. As will be seen, the package engineering team for microwave and millimeter-wave applications must have talents in material science, electromagnetics, heat transfer, manufacturing, test, and failure analysis.

11.1.1 Careful System Architecture and Solid Specifications

In many regards, this is the most important step on the development process due to the fact that this step determines the path that the product development will take. Metaphorically speaking, product development is like the sailing of a great ship at sea. It is important to get started along a path, any path. Otherwise, the ship stays moored to the dock. However, if the ship starts to sail at full speed in the wrong direction, it will take significant effort to turn the ship in the right direction. For electronic packaging products, the two items with the most influence on the direction that the product development will take are the system architecture and the specifications.

If the system is not architected correctly, it will not perform properly, and without specifications it is not possible to judge success or to know when the development stage is completed. The system architecture is often developed in parallel with the specifications and customer expectations. Fundamentally, it seems that product development should not move very far forward without a set of solid specifications. Nevertheless, it is amazing how many product developments do so without a written specification. Without a specification, it is impossible to know if your product will meet requirements, since there are none.

A poorly written specification, however, can be even worse than no specifications at all, because it gives the product development team the misguided confidence to move forward with product development. In the end, a hastily and poorly written specification will waste money and time. It is surprising how easy it is for a product development effort to get stuck in an engineering loop because no one in the organization is able to point to specifications that let

them know they have achieved the desired goals. Development costs and lost opportunity costs can be significant if proper requirements do not exist.

11.1.2 Proper Material Selection

Armed with a specification, the designer must choose the right materials to ensure reliability and proper functioning of the end product. For instance, the materials selected must not cause problems due to stress buildup. Even the most seasoned designer can overlook this problem. For most designs, extensive 3D mechanical modeling should be carried out to predict the stresses and strain over the required temperature range. The material set must also be analyzed to verify the reliability of the electronics being used. In other words, the junction temperatures of the electronic devices must be measured or simulated to verify that requirements are being achieved. For some high-power products, transient thermal simulations may be required. At a minimum, the product designer must verify that the materials chosen will not induce stress, will achieve the electrical bandwidth requirements, and will support the heat transfer requirements for reliable device junction temperatures.

11.1.3 Electrical Signal Integrity

The materials set often impacts the electrical bandwidth of the product. For the majority of designs, this requires the simulation of all transmission lines over the required frequency range or data rate (for high-speed digital signals). For example, a circuit that did not have the required data bandwidth was analyzed, and the cause of the reduced bandwidth turned out to be dispersion of the signal. This problem was not discovered until too late because an existing product was modified to have thicker substrates to reduce fabrication and assembly costs. The transmission lines were modified to maintain 50Ω impedance, but the circuits were not resimulated. The result was that the product had to be changed back to the previous substrate thickness.

Another mistake that has been made is performing limited signal integrity simulations and purposefully choosing not to analyze portions of a circuit. This often occurs when portions of a circuit are assumed to have a benign effect on electrical performance. This particular mistake occurs frequently. Unfortunately, this type of mistake is an epidemic for small- to medium-size IC developers. Many months of careful IC design are performed and the IC is released to fabrication without verifying that the IC can be packaged. The result all too often is that the IC cannot be properly packaged because the I/O cannot be connected in a fashion that maintains the proper functioning of the electrical signals. Therefore, electrical signal integrity simulations must be performed on all portions of the product.

11.1.4 Thermal Management

Thermal management is more than just proper material selection. It also includes all aspects of the packaging such as the thermal path for proper heat transfer, heat sinks, cold plates, cooling fans, temperature sensors, and circuits that monitor and control thermal management. For many product designs, the packaging engineer must have knowledge of the thermal interface that will be used in the next level in the system.

11.1.5 Proper Electrical Modeling

Modern electrical modeling tools have improved significantly during the past 25 years. The packaging designer must be able to properly use 3D electromagnetic analysis tools or have access to this capability.

11.1.6 Proper Mechanical Modeling

Mechanical modeling is important because it allows for checking proper fit and interfacing. Also, mechanical models can be used as inputs for stress, heat transfer, and electromagnetic analysis. In fact, for many design processes, the mechanical models are the configuration control and all results from analysis and design changes are incorporated into the mechanical model. The sophistication of mechanical modeling tools can automatically adjust the designs to account for different fabrication technologies. For instance, mechanical design software programs can be programmed to automatically adjust the dimensions of a sheet metal housing to account for bending effects. This level of sophistication can eliminate errors and improve the likelihood of a smooth transition into manufacturing.

11.1.7 Design for Manufacturing

One benefit of detailed mechanical models is that they can be used to generate fabrication-ready drawings. For designing into ceramic and laminate circuit boards, the manufacturers provide design rules that will guide the proper layout to ensure manufacturability. The next level of manufacturability is for the microelectronic assembly. For modules, there are rules for deep access wire bonding, component placement, wire bond pad size and location, epoxy squeeze-out requirements for component attachment, and other requirements. The best way to understand these requirements is to spend time on the manufacturing floor. There is no substitute for standing next to the person who programs and runs the automatic wire bonder or pick-and-place machine and asking what typical issues are encountered and how to avoid them. This opportunity is not always possible, but be sure to take advantage of it if it is.

11.1.8 Design for Testability

Products must be designed for testability. This includes testability for proper functioning at the design verification stage, reliability testing, burn-in, accelerated life testing, production-level testing (which may include programming of functions), and built-in test functions. The impact on electronic packaging is in providing access to test fixtures, test probe heads, heat transfer for test fixtures, and other electrical connections.

11.1.9 Production Process Transition

The transition to volume production requires the engineer to understand manufacturing processes and the particular product being produced. This is especially true for millimeter-wave products that have very tight tolerances in critical locations.

11.1.10 Proper Feedback from Field Failures

Each field failure is a gem of information that can lead to improvement. Of course, too many field failures and the product or company will not survive. It is all too easy to regard field returns as a glaring reminder of failure and therefore ignore them or not learn the valuable lessons they can teach. Proper analysis of field failures can improve the product by revealing manufacturing, test, and component issues. For instance, a product had a field return rate of about 0.3% which was judged by the company as a success. The failure analysis team included some of the design engineers who developed the product. It was found that the failure was due to a capacitor. Investigations showed that the capacitor had significant margin for its voltage and temperature. The team determined that the supplier of the capacitor had a reliability issue, which is common for capacitors. To resolve this issue, a new supplier for that capacitor was chosen.

11.2 Future for Packaging at Microwave Frequencies

As more and more products are developed for microwave bands, technology at these frequencies will become commodity items. This has certainly occurred to a large degree in the frequency bands below 6 GHz due to the wireless connectivity and mobile phone products. This will result in much lower costs, more component choices, and a larger installed base of manufacturers who are able to support volume production of products at these frequencies.

11.3 Drive for Lower Cost Packaging at Millimeter-Wave Frequencies

Until very recently, millimeter-wave frequency products were dominated by high-cost, finely machined metal products. Most of the systems were based on waveguide components. The cost of the ICs used in these systems was very high since systems were dominated by boutique IC processes such as indium phosphide (InP) and gallium arsenide (GaAs) MMICs. These high-cost ICs, combined with the tight machining tolerances required, justified the cost of these millimeter-wave components and systems. Although this is still true for many products, advances in SiGe and Si CMOS processing will drive down the cost of millimeter-wave packaging and products. Amplifiers and highly functional integrated circuits have been fabricated at 60 and 90 GHz [1–4]. The cost of SiGe and Si CMOSs is 10 times lower, or more, than for InP and GaAs processes. The usefulness of Si CMOS at millimeter-wave frequencies is due to the ever shrinking transistor gate lengths, which have increased the cutoff frequency. A transistor's cutoff frequency, ft, is a figure of merit for the transistor bandwidth. Higher ft means a transistor can operate at higher frequencies. Production Si CMOS processes are achieving transistor cutoff frequencies of more than 200 GHz for 90-nm processes and 400 GHz for 32-nm processes. The desire for small devices for mobile phones and higher performing computer processors has driven the need for small gate dimensions. The side benefit is that the Si CMOS devices are now useful for millimeter-wave applications. The availability of these low-cost processes and the resulting low-cost ICs are motivating the need for much lower cost packaging [5]. For many products, the future for millimeter-wave products will be highly functional ICs with cost targets similar to those of low-frequency Si ICs. This will drive the need for innovation in packaging to achieve the cost targets.

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Appendix A

A.1 Scattering Parameters

Any linear multiport network can be represented by S-parameters. The elements of a scattering matrix contain the coefficients that are unique for a particular network. They are a very useful analytical tool for the examination of microwave and millimeter-wave networks. Figure A.1 shows the linear network with the incident and scattered waves. The waves are phasor quantities and are defined as

$$a_k = \frac{V_k^+}{\sqrt{Z_{0k}}} = I_k^+ \sqrt{Z_{0k}} \tag{A.1}$$

$$b_k = \frac{V_k^-}{\sqrt{Z_{0k}}} = I_k^- \sqrt{Z_{0k}} \tag{A.2}$$

Where:

a_k = incident wave

b_k = scattered or outgoing wave and may include some effect from the incident wave on the other ports

V_k^+ = incident voltage wave

V_k^- = scattered voltage wave

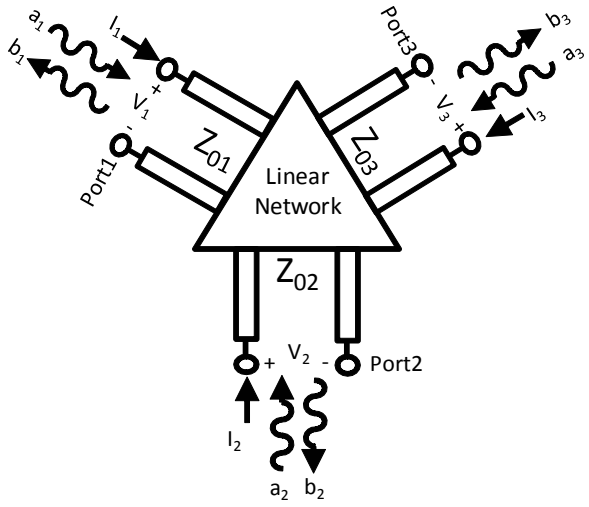

Figure A.1 A three-port linear network and the incident and scattered waves.

I_k^+ = incident current wave

V_k^- = scattered current wave

Z_{0k} = characteristic impedance of the line connected to port k.

A set of equations based on the scattered and incident waves that uses scattering parameters as the coefficients can be defined as

$$\begin{aligned} \mathbf{b}_1 &= S_{11}\mathbf{a}_1 + S_{12}\mathbf{a}_2 + S_{13}\mathbf{a}_3 \\ \mathbf{b}_2 &= S_{21}\mathbf{a}_1 + S_{22}\mathbf{a}_2 + S_{23}\mathbf{a}_3 \\ \mathbf{b}_3 &= S_{31}\mathbf{a}_1 + S_{32}\mathbf{a}_2 + S_{33}\mathbf{a}_3 \end{aligned} \tag{A.3}$$

However, (A.3) is just a set of linear equations with vectors and {b}, so that (A.3) can be rewritten as

$$\{\mathbf{b}\} = [S]\{\mathbf{a}\} \tag{A.4}$$

Where the scattering matrix is given by

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{A.5}$$

A.2 Impedance Parameters

The impedance parameters of a network describe a linear network. Figure A.2 shows a two-port network with port voltage and currents. The voltages and currents for an arbitrary *N*-port network are related to each other by the impedance matrix

$$\begin{bmatrix} V_1 \\ V_2 \\ \\ V_N \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & & Z_{14} \\ Z_{21} & & & \\ & & & \\ Z_{N1} & & & Z_{NN} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \\ I_N \end{bmatrix} \tag{A.6}$$

The elements of the impedance matrix can be found by

$$Z_{ij} = \left. \frac{V_i}{I_j} \right|_{I_k = 0 \text{ for all } k \neq j} \tag{A.7}$$

One method to ensure that all the currents are zero except the current I_j is to open all of the other ports. In other words, (A.7) can be understood as opening all the other ports except at port j, then driving port j with current I_j and measuring the resulting voltage V_i. From this, Z_{ij} is computed.

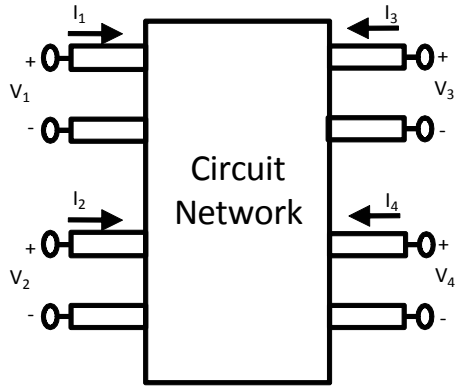

Figure A.2 A four-port network and with port voltage and currents defined.

Appendix B

B.1 Multilayer Transmission Line Tool

The quasistatic variational technique was used to develop an analysis program that predicts the line impedance, effective dielectric constant, electrical length, delay, line capacitance, and line impedance of a zero thickness transmission line in a multilayer structure. The input units are inches (1 inch = 25.4 mm). The program assumes that there are four dielectric layers, two above and two below the signal line. However, it is possible to analyze transmission lines with fewer than four dielectric layers. As shown in Figure B.1, there are three input fields for the analysis.

B.2 Physical Parameters

In this portion of the program, the physical description of the transmission line is input. The inputs are the thickness of each substrate layer, the line width of the conductor, the cavity width, and the length of the line. For transmission lines with fewer than four dielectric layers, it is possible to use the software. Figure B.2 shows how to divide up—for analysis only—the dielectric layers of the physical configuration to be analyzed. For stripline, the dielectric above and below the strip are divided so that there are four sections. The thicknesses and dielectric constants are input into the appropriate fields.

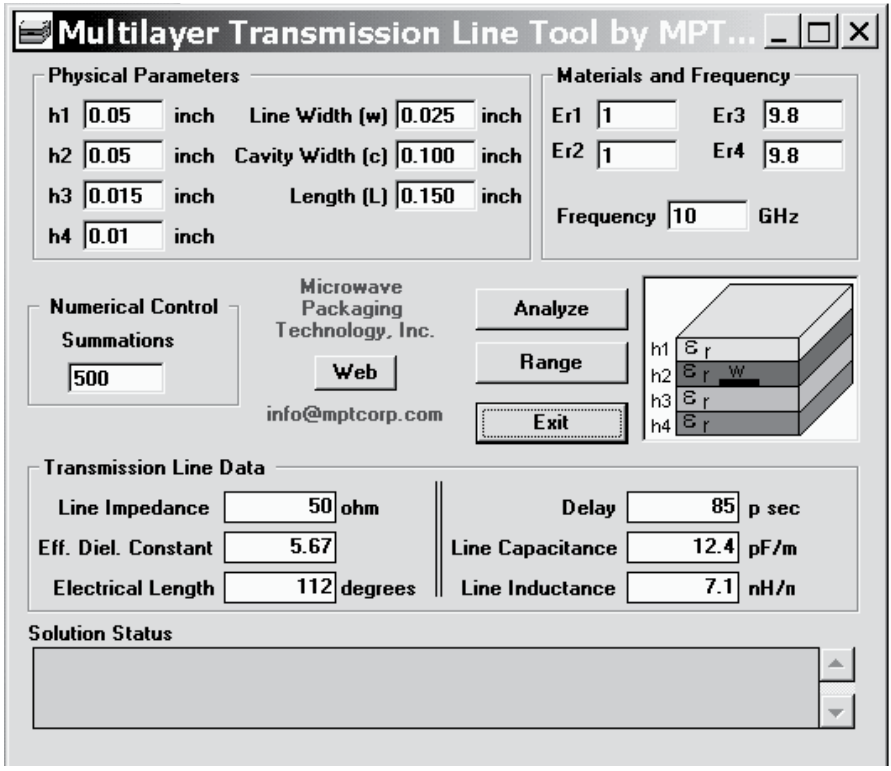

Figure B.1 Screen shot of a transmission line analysis software tool that is based on the quasistatic variational method.

B.3 Numerical Control

The software is based on a numerical summation. To add another layer of control to the user, the number of summations can be input. For most transmission lines, 500 to 1000 summations will be enough. It is possible to monitor the line impedance as a function of the number of summations to verify that the solution has converged.

B.4 Analysis

By pressing the analyze button, the analysis starts and the transmission line data fields are populated with the updated values. The solution status window can be used to monitor the solution speed. For modern computers, the solution speed is so quick that monitoring the solution status is not needed.

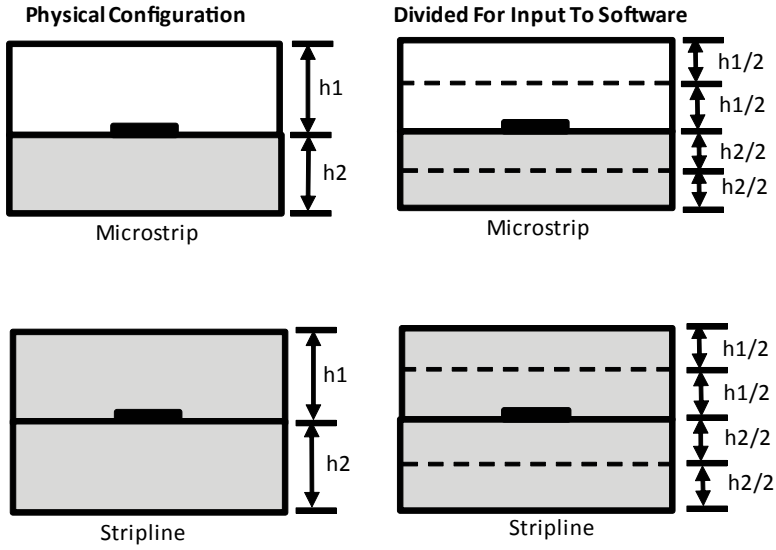

Figure B.2 Illustration of how transmission lines with fewer than four dielectric layers can be analyzed.

Appendix C

C.1 Thermal Calculator Software Tool

A simplified thermal calculator based on the analysis method in Section 9.5 has been implemented in a computer program. The program predicts the temperature drop across multiple layers of a material system with up to six layers. Each layer is defined for its thermal conductivity and thickness. The heat source can be either an electronic component or an ideal heat source. The program allows the spreading angle to be either 45 degrees for every layer or zero degrees for every layer. The mounting temperature is defined as the *base temperature*. The result is the temperature at each the interface between each layer and the device maximum junction temperature. The computer program is illustrated in Figure C.1. Operation of the program is straightforward and requires three steps.

Step 1: Describe the Heat Source

In this step, the user must define whether the heat source is an electronic component or an ideal heat source. If it is an electronic component, then the user must specify the power dissipated, the junction to case thermal resistance, and the thermal area of the heat flux. For a bare die, the thermal area is normally taken to be the area of the die. For a package part, such as a QFN, the thermal area would be the die paddle on the bottom of the package. For an ideal heat source, the thermal area is just the area of the heat source.

Step 2: Describe the Materials

In this step, the materials that make up the material system are defined. Up to six material layers can be specified. Use the check boxes to select the number of

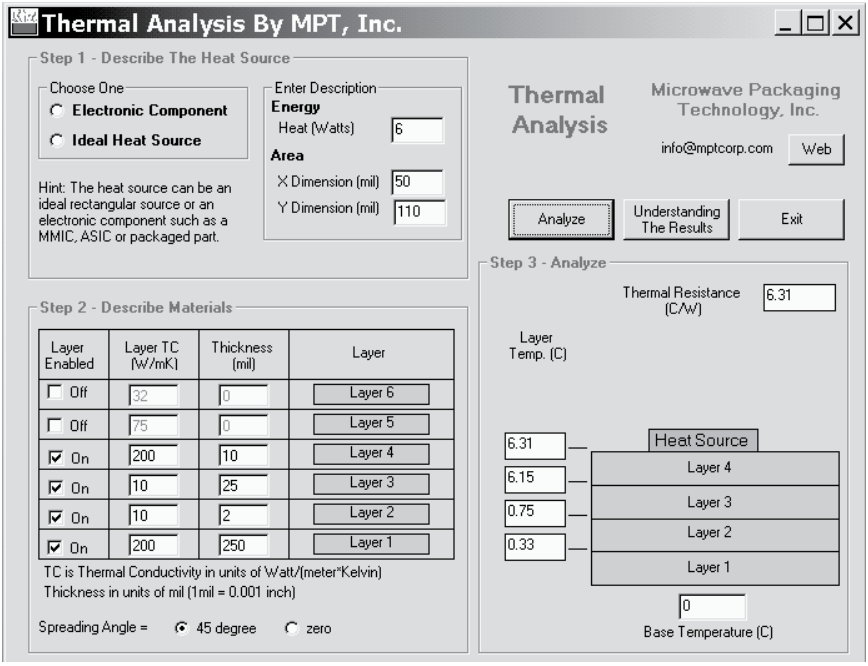

Figure C.1 Screen shot of the thermal analysis software program.

layers in your design. For each layer, specify the layer thermal conductivity in units of W/mK and the thickness in units of mil (1 mil = 0.001 inches = 0.0254 mm). Also, at the bottom of the box for Step 2, the spreading angle is selected. The two options are 45 degree and zero degree heat spreading. Zero degree heat spreading is more conservative.

Step 3: Analyze and View Results

Since this method uses closed form equations, the analysis is nearly instantaneous. Press the Analyze button to start the analysis. If an electronic component is chosen in Step 1, then the analysis result shows the device junction temperature. If an ideal heat source is specified, then the thermal resistance of the material stack is calculated.

Error Codes

The software has some error catching. For instance, if something other than a number is input in one of the data fields, the program will catch the error and provide a warning. If an error 88 occurs, it is best to restart the program.

About the Author

Rick Sturdivant has 24 years of industry experience designing products for microwave and millimeter-wave systems. He earned an M.S.E.E. from UCLA, a B.S.E.E. from CSULB, and a B.A. in religion from Vanguard University. He is the author of Chapter 1 of *Microwave Electronic Packaging* (Springer Publishing, 2010). He was a Hughes Aircraft Microwave Fellow from 1990–1992. He developed the world's first tile array module for phased array radar, for which he received the Engineering Excellence Award in 1993 from Hughes Aircraft Company. He was part of a team that developed the world's first ball grid array modulator driver in 2002. He has started several successful companies that develop products for consumer electronics, wireless, and military systems. He is currently president of Microwave Packaging Technology, Inc., which provides research and development services in the area of phased arrays for communication and radar systems. He has been a technical reviewer for the *IEEE Microwave Theory and Techniques* and for the IEEE International Microwave Symposium, past chair of the MTT-S Local Chapter in Los Angeles, and a current member and a past chair of the IEEE MTT-S Technical Committee on Microwave and Millimeter-wave Packaging. He has published over 20 technical articles and holds five patents with three others pending.

Index

2.5D simulators, 223
Absorber, 10
Advanced thin-film techniques, 73, 77–78
Air cavity packages
  defined, 144
  illustrated, 145
American Society for Testing and Materials (ASTM) manuals, 63
Amplifier efficiency, 203–5
Anisotropic dielectric constant, 45–46
ANSYS, *xvii*
Antennas, wire bonds as, 125–26
Arrhenius equation, 205–8
Atomic polarization, 42

Bake-out, 93
Ball-and-stitch wire bonding, 120
Ball bonds, 109
Ball grid array (BGA), 158

Capacitance
  distributed, microstrip lines, 173
  equivalent circuits, 186
  and inductance matrix method, 147–51
  microstrip line and stripline transition, 185–87
  parasitic, 185
  stray, 187
Capacitors
  performance and operating frequency, 5–6
  reactance, 4–5
  real versus ideal comparison, 6
Cavity mode, avoiding, 176–77
Cavity resonance method, 51–52
Cavity resonances, 51–52, 176–77, 194
CBCPW to microstrip transition, 183, 184
Ceramic packaging
  advanced thin-film techniques, 77–78
  benefits of, 67–88
  high-temperature cofired ceramics (HTCC), 68, 82–86
  low-temperature cofired ceramic (LTCC), 86–87
  thermally enhanced thick-film processes, 82
  thick-film ceramics, 78–82
  thin-film ceramics, 69–77
Ceramics
  history of, 68
  in rf products, 67
  thin-film, 68, 69–77
Ceramic substrate, 81
Characteristic impedance
  even-mode, 25
  modeling of, 11
  odd-mode, 24–25
Circuit boards (laminate)
  alignment and lamination, 94
  artwork generation, 93
  bake-out, 93
  clean layers, 93
  cost modeling, 97–98
  database review and acceptance, 92
  drill and deburr, 94
  electrical testing and inspection, 96
  fabrication of, 92–96

Circuit boards (laminate) (continued)
finish plating, 95
line width and gap tolerances, 99
oxide treatment of inner layers, 93–94
pattern and etch, 93
process flow, 92
silk screen and CNC routing, 96
solder mask, 95
thickness, 100–101
through-hole plating, 94–95
tolerances, 98–101
via catch pads, 99–100
Circuit elements
inductance and capacitance matrix model, 147
three-dimensional packaging as, 196
CNC routing, 96
Coaxial lines, 15, 18, 19
Coefficient of thermal expansion (CTE), 61, 209
Cofired ceramic microstrip to stripline transition, 183–89
Cofiring layers, 85–86
Complementary metal-oxide semiconductor (CMOS), 30
Compressible connectors
formations, 192
goal for, 191
height, diameter, and spacing between, 192–93
illustrated, 192
impedance of, 193
parasitic effects, 193
transitions between motherboards and, 193
without dielectric header, 191
Conductor-backed coplanar waveguide (CBCPW), 18, 19, 162–67
analysis of, 163
CPW comparison, 162
defined, 162
design guidelines, 167
dominant modes, 165
drawback, 163
effective dielectric constant, 163
with ground vias, 166
illustrated, 162
impedance and effective dielectric constant comparison, 164
impedance design equations, 163
parallel plate mode, 165–66
slot line mode, 165
transmission line thickness, 163–64
Conductor loss, 13–14, 16, 17
Convection, 202–3
Coplanar waveguide (CPW), 103–4
conductor-backed (CBCPW), 162–67
configurations, 135
line impedance, 134
proximity effect, 136
Cost of laminates, 96–98
drivers, 96–97
modeling, 97–98
Coupled lines, 24, 25
Coupled-π model method, 151–57
EM simulator, 153, 155, 156, 157
inductors with magnetic coupling, 151
return loss and insertion loss comparison, 153
schematic of package interconnect, 153
Coupling, 21–26
at lower frequencies, 23
magnetic, 151
simulated, 26
between transmission lines, 23, 24

Design for manufacturing, 236
Design for testability, 237
Dielectric constants, 41–46
anisotropic, 45–46
effective, 49, 50, 163
materials permittivity and, 44
measurement of, 47–56
as tensor, 45
Dielectric loss tangent, 46–47
Dielectric material
anisotropy of, 46
with electric field, 42, 43
waveguide filled with, 52
with zero voltage, 42
Dispersion effects
defined, 20
in microstrip, 21
reduction, 22
Dissipated thermal power, 203–5
Distributed effects, 4–29
coupling and cross-talk, 21–26
dispersion effects, 20–21
in lumped elements, 4–6

parasitic and grounding concerns, 26–29
transmission lines, 10–19
undesired resonances, 6–10
Distributed parallel plate capacitance, 173
Domain decomposition method (DDM), 223, 230
Drill and deburr, 94

Effective dielectric constants, 49, 50, 163
Electrical modeling, 236
Electrical parameters, 41–58
dielectric constant, 41–46
loss tangent, 46–47
metal electrical conductivity, 56–58
Electrical supply integrity, 235
Electromagnetic modeling. *See* EM modeling
Electromagnetic stimulator, 134
Electronic packaging
ceramic, 67–88
common metals used in, 14
conclusions, 34–35
coupling and cross-talk, 21–26
defined, 2
dispersion effects, 20–21
distributed effects, 4–29
first-level interconnects (FLIs), 31–33, 107–40
future for, 237
heat transfer, 201–17
at higher frequencies, 3
introduction to, 1–35
keys to success, 234–37
laminate, 91–105
lower cost, drive for, 238
lower frequency circuits, 2–3
lumped elements distributed effects, 4–6
materials, 39–64
modules, 34
ohms per square, 57
parasitic and grounding concerns, 26–29
second-level interconnects (SLIs), 33–34, 143–59
thermal effects, 29–31
transmission lines, 10–19
undesired resonances, 6–10
EM modeling, 219–31
defined, 219
domain decomposition method (DDM), 230
finite difference time domain (FDTD) method, 228–29
finite element method (FEM), 228
goal of, 219
integrated methods, 229–30
method of moments (MoM), 166, 222, 223, 227–28
mode matching technique, 229
quasistatic simulation of transmission lines, 223–26
See also EM simulators
EM simulators
2.5D, 223
field, 223
insertion phase results comparison, 157, 158
isolation results comparison, 157
Maxwell's equations, 219–20
model element values, 155
MoM-based, 227–28
nonphysical results, 221–22
planar mesh, 220
port impedance prediction, 222
problem setup, 220–21
process flow, 221
results, checking, 221
return loss and insertion loss results, 153, 155, 156
same structure on different simulators, 222
schematic, 156
Emulsion, 81
Equivalent circuits
capacitance, 186
insertion loss, 29
microstrip line and stripline transition, 188
in parasitic and grounding concerns, 29
series inductance in, 175
Etching, 81
Even-mode characteristic impedance, 25

Feedback from field failures, 237
Field effect transistors (FETs), 30–31
Field failures, feedback from, 237
Filled waveguide method, 52–54
Finish plating, 95

Finite difference time domain (FDTD) method, 222, 228–29
Finite element method (FEM), 222, 228
First-level interconnects (FLIs), 31–33, 107–40
  defined, 31
  flip chip, 126–39
  illustrated, 32
  at millimeter-wave frequencies, 107
  ribbon bonding, 126
  types of, 32
  wire bonds, 31–32, 107–26
Flip chip interconnects, 126–39
  bump pad effect, 130
  challenges, 126–27
  defined, 126
  electrical modeling of, 129–35
  hard bump, 128, 129
  parameters, 130
  parasitic modes in, 135–39
  solder bump, 128, 129
  stud bump, 128–29
  substrate proximity, 131
  thermal concerns for, 139
  transition illustration, 130
  types of, 128–29
  See also First-level interconnects (FLIs)
Frame, 80
Frequency band designations, 2
Future for packaging, 237

GaAs MMIC transmission line, 144, 146
Galerkin technique, 227
GaN high-power amplifier, 209, 211
GaN transmit/receive module, 34
Grounding
  peripheral bumps, 138
  vias for, 175–76

Hard bump flip chip interconnect, 128, 129
Heat dissipation, 29–30
Heat transfer, 201–17
  amplifier efficiency and, 203–5
  conclusions, 216
  convection, 202–3
  junction temperature, 208–9
  junction temperature with multiple material layers, 209–12
  mechanisms, 201–3
  radiation, 203
  reliability and, 205–8
  thermal conductivity, 202
  thermal simulations using FDM, 213–15
  thermal simulations using Spice, 212–13
High Frequency Structure Simulator (HFSS), *xvii*
Highly integrated modules with vertical transitions, 195–96
High-performance laminate materials, 101–2
High-temperature cofired ceramics (HTCC), 68, 82–86
  defining characteristic, 83
  furnace, 86
  parts illustration, 87
  postprocessing, 86
  punching, 84
  slurry, 83–84
  stacking, pressing, and cofiring, 85–86
  tape casting, 84, 85
  use of, 82
  via filling and conductor printing, 85
Hybrid circuit model
  application of, 158–59
  basis, 158
  defined, 157–58

Impedance parameters, 243
Incremental inductance, 14
Inductance and capacitance matrix method, 147–51
Insertion loss
  determination, 54–55
  EM simulator, 153, 155, 156
  of package equivalent circuit, 29
  simulated, 26
Integration methods, 229–30
Ionic polarization, 42
Isolation, vias for, 175–76

Junction temperature
  across each layer, 212
  device, 208–9
  finding, 209
  maintaining, 208
  manufacturer specification, 209
  with multiple material layers, 209–12

Kirchoff's current law, 147
Kirchoff's voltage law, 147

Laminate board microstrip to stripline transition, 189–90
Laminate multichip modules (MCM-Ls), 103–4
Laminate packaging, 91–105
  artwork generation, 93
  bake-out, 93
  board fabrication, 92–96
  board tolerances, 98–101
  clean layers, 93
  conclusions, 104
  cost of laminates, 96–98
  high-performance materials, 101–2
  laminate multichip modules, 103–4
  liquid crystal polymer (LCP), 102–3
  pattern and etch, 93
  process flow, 92
Laminates, cost of, 96–98
Lange coupler, 21
LCR matrix method, 151, 153
Lid effect, 176–77
Line impedance, 11–12
  CPW line, 134
  differentiation of, 16
  wire bonds, 117–18
Liquid crystal polymer (LCP), 102–3, 144
  applications for, 103
  benefits of, 102–3
  defined, 102
Longitudinal section magnetic (LSM) mode, 8, 177
Loss tangents, 46–47
  dielectric, 46–47
  measurement of, 47–56
Lower cost packaging, drive for, 238
Low-temperature cofired ceramic (LTCC)
  characterization, 86
  fabrication process, 87
  metal systems for, 87
  substrate fabrication, 34
Lumped elements
  defined, 4
  distributed effects, 4–6

Manufacturing, design for, 236
Materials, 39–64
  electrical parameters, 41–58
  energy bands of, 41
  mechanical parameters, 58–63
  overview, 39–40
  parameters, unknown, 40
  PCB, measured data, 46
  selection of, 235
  top-level view of selection process, 40
Maxwell's equations, 43–44, 219–20
Mean time to failure (MTTF)
  applications and, 207
  defined, 205
  determination of, 205–6
  at elevated temperature, 206
  maximum junction temperature and, 208
  plot, 207
  reaction rate and, 206
Measurement of dielectric constants/loss tangents, 47–56
  cavity resonance method, 51–52
  filled waveguide method, 52–54
  ring resonator method, 47–51
  space-free methods, 56
  transmission line measurement, 54–55
Mechanical modeling, 236
Mechanical parameters, 58–63
  stress and strain, 61
  thermal conductivity, 58–60
  thermal expansion, 60–61
  Young's modulus, 61–63
Mesh, 80
Metal electrical conductivity, 56–58
Metal pattern, 81
Metals, in electronic packaging, 14
Method of moments (MoM), 166, 222, 223
  defined, 227
  simulators, 227–28
Microstrip line and stripline transition
  cofired ceramic, 183–89
  design parameters, 184–85
  HFSS modeling, 188
  illustrated, 184
  laminate board, 189–90
  overview of, 183–84
  See also Transitions
Microstrip lines, 18, 19
  CBCPW transition to, 183, 184
  design of, 171–75
  distributed capacitance, 173

Microstrip lines (continued)
equivalent circuits, 188
lengths of, 55
multiple layers, 189
parameters, 173
port field distribution, 172
propagating regimes, 171
surface wave modes, 171–72
tolerances, 99
transverse higher order mode, 172
use in modules and motherboards, 171
Microwave hybrids, 7–8
Microwave integrated circuits (MICs), 7
Mode matching technique, 229
Modules, 34
Motherboards
compressible connector transitions, 193
dielectric header termination at, 194
microstrip lines use in, 171
Multilayer transmission line tool, 245–47
analysis, 246–47
defined, 245
numerical control, 246
physical parameters, 245

Odd-mode characteristic impedance, 24–25
Ohms per square, 57
Organization, this book, *xv–xvi*
Orientation polarization, 42
Oxide treatment of inner layers, 93–94

Packaging engineers, 2
Parameters
electrical, 41–58
flip chip interconnects, 130
impedance, 243
mechanical, 58–63
microstrip lines, 173
physical, 245
scattering, 241–42
Parasitic and grounding concerns, 26–29
Parasitic resistance, 27
Physical parameters, 245
Physical vapor deposition (PVD), 73, 74
Postprocessing, 82, 86
Power added efficiency (PAE), 204–5
Pressing layers, 85–86
Printed circuit boards (PCBs), 33, 44
Printing machine, 81
Production process transition, 237
Propagation constant, 8–9, 11
Proximity effect, CPW IC, 136
Pseudo-random binary sequence (PRBS) signal, 20
Punching, 84

Quad flat no-lead (QFN)-style package
defined, 143
EM simulator insertion phase results, 157, 158
EM simulator isolation results, 157
HFSS simulation results, 154
illustrated, 33, 143
with LCR matrix method, 152
return loss and insertion loss results, 153, 155, 156
thermal resistance of, 208
Quasistatic simulation of transmission lines, 223–26

Radiation, 203
Radio-frequency (rf), xvi
electronics in early systems, 1
pioneers of, 1
Rectangular waveguide resonator equation, 194
Reliability, heat transfer and, 205–8
Resonances
cavity, 6–7, 51–52, 176–77
effects with/without absorber, 11
quarter-wave, 138
undesired, 6–10
Resonant frequency
approximation by rectangular waveguide resonator equation, 194
first-order approximation, 8
Return loss, EM simulator, 153, 155, 156
Ribbon bonding, 126, 127
Ring resonator
fabricated, photo of, 50
illustrated, 47
measured data, 50
measurement method, 47–51
modeling, 48

Scattering parameters, 241–42
Screen, 80
Second-level interconnects (SLIs), 33–34, 143–59

coupled-π model method, 151–57
defined, 33, 143
electrical modeling of surface-mount packages, 146
hybrid circuit model, 157–59
inductance and capacitance matrix method, 147–51
packaging of, 33–34
Shrunk small outline package (SSOP), 159
Silk screen, 96
Skin depth, 12–13
Slurry, 83–84
Small outline package, 144
Solder bump flip chip interconnect, 128, 129
Solderless interconnects, 191
Solder mask, 95
Space-free methods, 56
Spice
comparison of units used for heat transfer simulation in, 214
defined, 212
Squeegee, 80
Stacked substrate solderless interconnects, 190–95
Stacking ICs and packages, 196–97
Stacking layers, 85–86
Straight wire bonds, 113–20
analyzed as ideal wire, 114
DC resistance, 118
equivalent circuit of, 115, 116
HFSS simulation of, 119
illustrated, 113–20
between substrates, 113–20
Strain
defined, 61
plot showing, 62
thin-film ceramics, 76
Stress
defined, 61
plot showing, 62
Striplines, 18, 19
catch pad area, 187
design, 168–71
design procedure, 170–71
high-order parasitic modes, 168
line impedance change, 101
microstrip line transition to, 183–89
selection of, 169
signal line thickness, 168
slot mode, 169
TEM mode, 168
thickness, 101
undesired modes, 169–70
Stud bump flip chip interconnect, 128–29
Successful packaging, 234–37
design for manufacturing, 236
design for testability, 237
electrical modeling, 236
electrical supply integrity, 235
feedback from field failures, 237
material selection, 235
mechanical modeling, 236
production process transition, 237
system architecture and specifications, 234–35
thermal management, 236
Surface-mount packages
electrical modeling of, 146
side view, 27
Surface-mount technology (SMT) packages, 161

Tape casting, 84, 85
Testability, design for, 237
Thermal calculator software tool
defined, 249
error codes, 250
illustrated, 250
operation steps, 249–50
Thermal conductivity, 58–60, 202
Thermal effects, 29–31
Thermal expansion, 60–61
Thermally enhanced thick-film processes, 82
Thermal management, 236
Thermal simulations, 212–13
electric circuit model, 213
with FDM, 213
with Spice, 212–13
Thick-film ceramics, 78–82
advantages, 78
defined, 78
drawbacks, 78–79
emulsion, 81
etching, 81
frame, 80
metal pattern, 81
paste, 79–80
postprocessing, 82

Thick-film ceramics (continued)
printing machine, 81
process illustration, 79
screen and mesh, 80
squeegee, 80
substrate, 81
thermally enhanced, 82
viscosity, 80
Thin-film ceramics, 68, 69–77
advanced processes, 73, 77–78
circuits, 74
illustrated, 75
metal thickness, 76–77
strain, 76
targets in physical vapor deposition, 73
Thin-film chamber, 72
Thin-film sputtering, 69–70
Thin-film substrate, 71
Thin-film vapor deposition, 74
Three-dimensional packaging
cost and complexity, 197
defined, 181, 190
design challenges, 197
example of, 190
highly integrated modules with vertical transitions, 195–96
integration by stacking ICs and packages, 196–97
package as circuit element, 196
stacked substrate solderless interconnects, 190–95
test and measurement, 197
Through-hole plating, 94–95
Tile array model, 190–91
Tolerances, laminate circuit board, 98–101
Transitions
bandwidth, 182–83
CBCPW to microstrip, 183, 184
cofired ceramic microstrip to stripline, 183–89
defined, 181
example of, 181
laminate board microstrip to stripline, 189–90
motherboards and compressible connectors, 193
between transmission lines, 181, 182–90
vertical, 195–96
Transmission line design, 162–75
conductor-backed CPW (CBCPW), 162–67
microstrip lines, 171–75
striplines, 168–71
Transmission lines, 10–19
attenuation constant, 12
characteristic impedance, 11
complex surface impedance, 16
conductor loss, 13–14, 16, 17
coupling between, 23, 24
illustrated, 12
incremental inductance, 14
insertion loss determination, 54–55
load impedance, 11
loss tangent, 17
measurement, 54–55
microstrip, 18–19, 21, 55, 99, 171–75
popular design, 162–75
propagation constant, 11
quasistatic simulation of, 223–26
skin depth, 12–13
skin effect, 12
source generator, 11
source impedance, 11
striplines, 168–71
with strip sandwiched between dielectric layers, 225
total insertion loss, 16
types of, 19
wire bonds as, 125
Transmission line transitions, 181, 182–90
Transverse electromagnetic mode (TEM), 102
Transverse higher order mode, 172
Traveling wave tube (TWT) amplifiers, 1

Undesired resonances, 6–10

Vector network analyzer (VNA), 147–48
benefit of, 147
measurement conducted using, 148–49
Vertical transitions, 195–96
Via catch pads, 99–100
Vias
fence structure, 175
for isolation and grounding, 175–76
use illustration, 176

Waveguide test system, 53–54
Wedge bonding, 109, 114
Wire bond pull tester machine, 110–11
Wire bonds, 31–32, 107–26
  as antenna, 125–26
  ball bonds, 109
  before/after pull testing, 111
  connection, 33
  cross-sectional view, 121
  DC resistance, 118
  equivalent circuit of, 115, 116
  in filters, 124
  as first-level interconnect, 107–8
  ground current parasitics, 122–24
  ground signal path, 124
  HFSS simulation of, 119
  illustrated, 109
  interconnects, 107–24
  line impedance, 117–18
  manufacturing, 108–10
  metallurgical bond, 108
  between MMIC and substrate, 120–22
  purpose of, 33
  reliability, 110–12
  RF uses, 124–26
  ribbon bonding with, 127
  series inductance and, 108
  straight, 113–20
  between substrates, 113–20
  as transmission lines, 125
  tuning, 124
  as tuning elements, 124
  wedge, 109, 114
  See also First-level interconnects (FLIs)

Young's modulus, 61–63, 75